Specification for the External Field Bank Module Capacitor Charge/Discharge Power Supply (CCDPS) for FLARE

March 10, 2016

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1 Specifications for External Field bank module

1.1 Description

Bank schematic is shown in Fig. 1. Starting on the left side of the figure, the module is charged by connecting both positive and negative supply lines. A power supply protection circuit is shown (although the components are distributed between the charge supply rack and the capacitor modules – please refer to the Charge Specification for details). A bleed resistor is connected in parallel with each capacitor and is used to slowly drain bank charge in case of failure of all other dumps (i.e. if left alone overnight the bank will passively discharge below the NFPA 70E safe approach threshold of 50 V). Before each shot, the dump load relays are opened. Then the charging relays are closed and the charging supply charges the caps. When the set-point is reached, the charging switches are opened. The capacitors are then discharged through the inductive and resistive load of the coil, and crowbarred with a delay corresponding to peak current. For EF, the first swing current will always be greater than zero so a uni-polar crow bar switch (i.e., diode commutation) will be used. Following a shot, the dump switch is closed to ensure the capacitors are fully discharged. Capacitor fuses are thin wires designed to blow during an over-current event. They will be used on each cap and will connect the capacitor to the busbar. Each of the components will be described in the following sections.

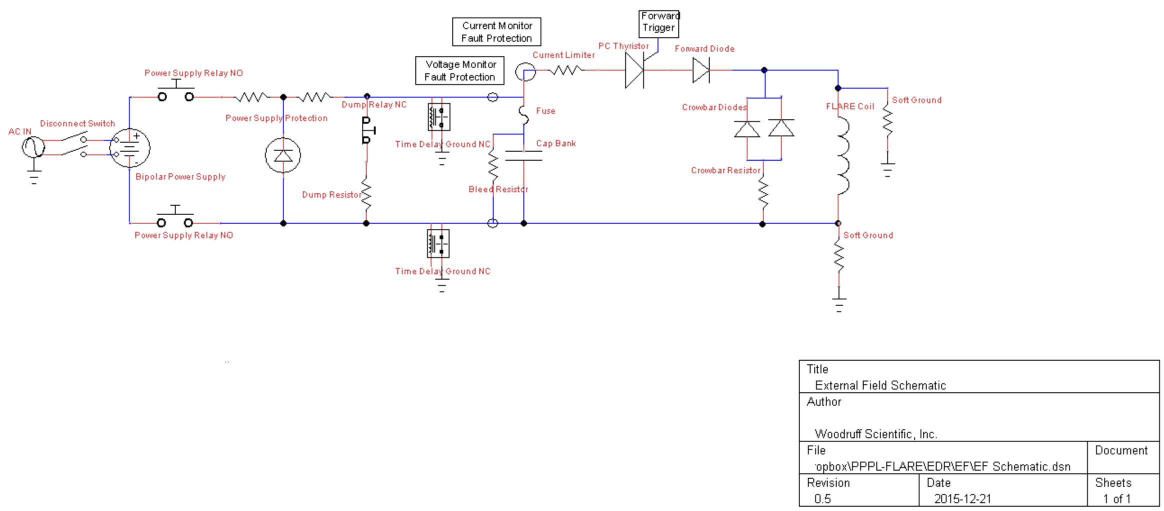


Figure 1: External Field Circuit Schematic

The EF bank module is designed to energize the EF coil set, providing a current pulse per Fig. 9, meeting the specifications in Table 1. The power supply system shall be designed for a minimum of 10 years design life and a minimum of 100,000 full power shots with regular maintenance.

	EF
# Sub-Coils	2
V (Volts)	1400
Imax (A)	26000
Day 1	33.3
Peak I (kA)	26
trise (ms)	> 30
tcrowbar	Peak
Swing Imin	+ve

Table 1: Target parameters for EF bank

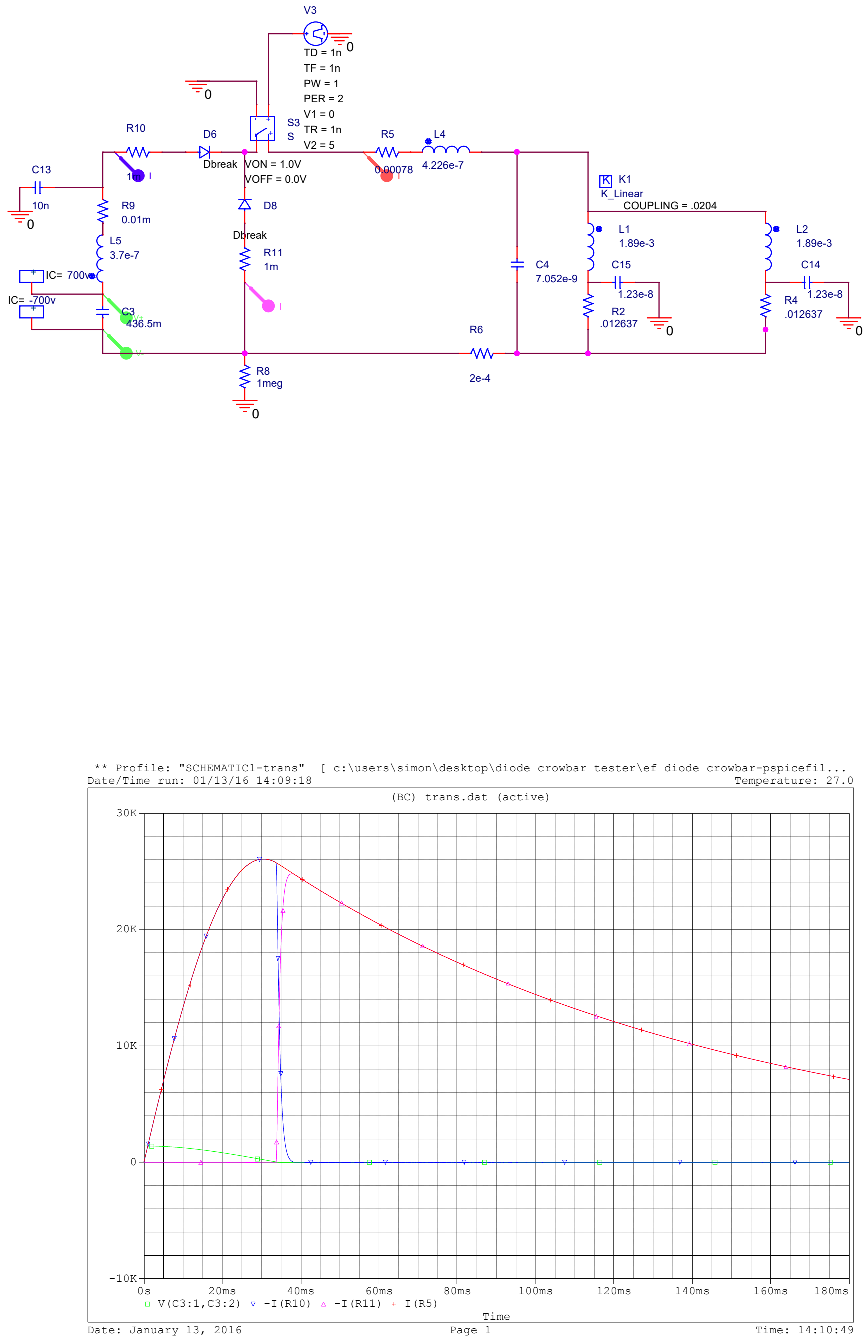


Figure 2: PSpice External Field Schematic and Analysis

1.2 Full Assembly: module

Fig. 3 shows the full bank assembly mounted on two 48 inch square steel pallets.

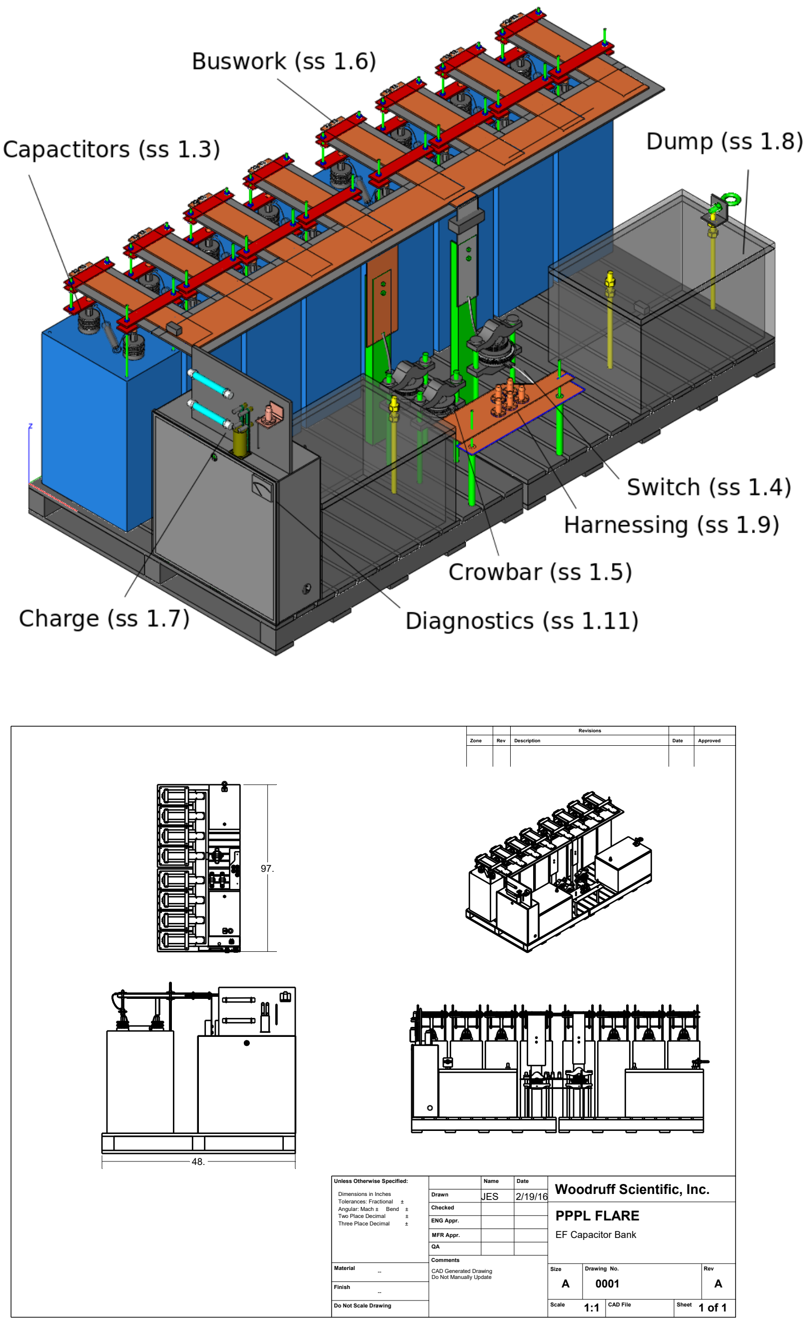


Figure 3: Engineering design point for bank module

The full assembly must not have a footprint greater than 32sqft with a maximum of 64sqft for egress and maintenance, and must be engineered as a module that can be transported and installed on-site with only a small number of connections (connections for 110V power, etc). The EF Bank and all related components will be mounted on 2 48"x48" standard pallets, total height under 50 inches, total weight per pallet of 1200lbs. Assembly instructions will be provided separately.

1.3 Capacitors

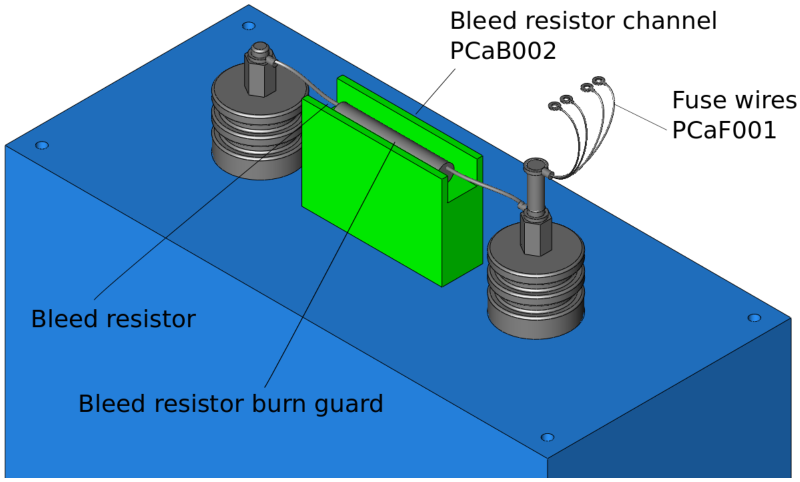


Figure 4: Capacitor detail

The capacitors will not experience voltage reversal as diodes are used in the crowbar circuit and protecting the forward switch. Each capacitor unit should be individually fused and self-protected. Energy dumping resistor(s) shall be specified for safe dissipation of stored energy (see below). The dissipation time should be limited to the shorter of the relevant industrial standards or the experimental needs. The EF bank will use 8 NL55650-1.4KV Capacitors, by Richardson Electronics. They have a rated capacitance of 55650uF and a rated voltage of 1.4kVDC. They are rated for 0% discharge voltage reversal. The capacitors are expected to survive at least 500,000 full power shots without failure, per cap manufacturer specification see appendix for the Richardson specification. In parallel with each capacitor is a bleed resistor. These are a redundant dump mechanism for the stored energy. These resistors are sized to discharge the bank to below 50 volts over 12 hours. The bleed resistors are a passive "last resort" safing mechanism in case of failure of the water dump or loss of buswork connections, allowing the operator to leave the bank overnight to dissipate its stored energy. The bleed resistor shown in Fig. 4 is a 25W 700kΩ Ohmite Mox-G (see spec in appendix). Shown also in Fig. 4 are the fuse wires, which are 4 15AWG bare copper wires. Burn guard will be mounted to the cap with double-sided adhesive tape (e.g. 3M Command Strips).

1.4 Forward Switch

The forward switch for the EF circuit is a 5STP 50Q1800 phase control thyristor manufactured by ABB Semiconductor. The thyristor can be trigger by a TTL compatible signal which will be generated by a fiber optic frequency to voltage converter. A diode is used to protect the forward switch. Switches and diodes are connected to buswork with 1/2 inch copper braid and ring terminals.

1.5 Crowbar Switch

The crowbar for the EF bank modules consists of a parallel stack of 2 diodes (see Fig. 6) with part number 5SDD 60N2800 manufactured by ABB Semiconductors. After the forward switch is fired, the diodes will not conduct until the current peak is reached effectively crowbarring the circuit at maximum current.

1.6 Buswork

Buswork consists of busbars connected to the caps by use of brass adapters that are secured by 1/4-20 bolts and have knife-edges that will bite into the copper busbars (see detailed call-out in Fig. 7. A larger bus is used to interconnect all the smaller capacitor buses which then feeds into the current limiting stainless steel resistor. Outgoing and return busbars are isolated from each other by use of multiple layers of mylar

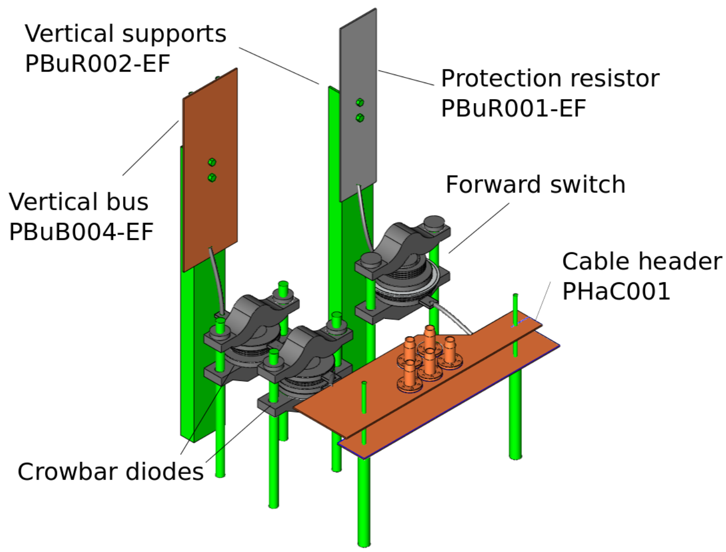


Figure 5: Forward switch and crowbar diodes for the EF bank.

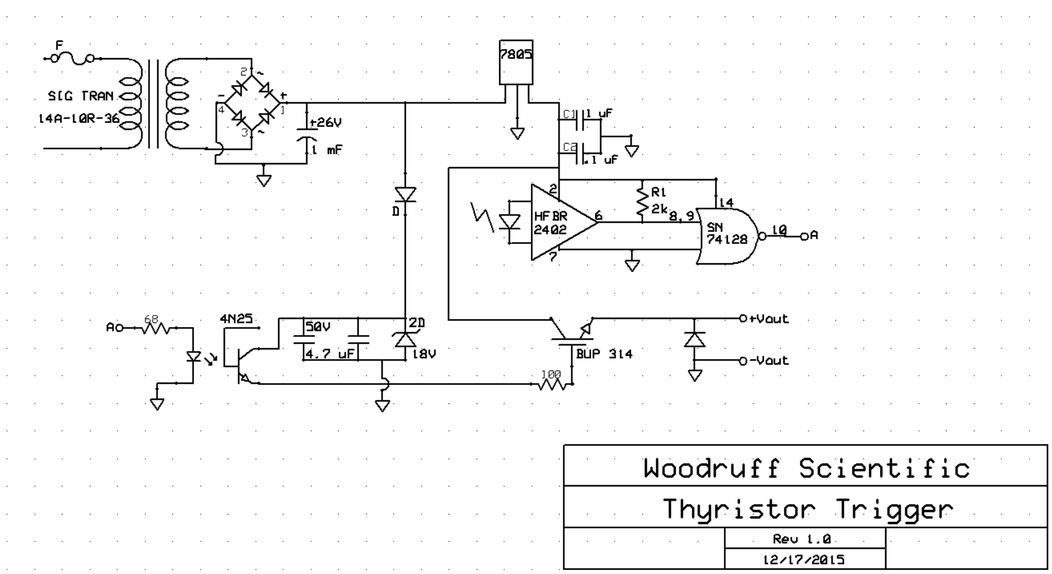


Figure 6: Fiber to Voltage Thyristor Trigger

sheet, with sufficient overhang to meet the 2E+1 stand-off requirement. A 1mOhm overcurrent protection resistor is provided in case of short failure, clamping the maximum current to tolerable thresholds for the caps. The power supply should be properly insulated based on design. The rule of thumb to be followed is 2E+1, where E is the maximum system voltage. All bus work should be taken into consideration so that the inductance does not limit the system performance.

1.7 Charging

The charging supply will consist of two TDK-Lambda supplies, one 402L-10kV-POS-208VAC and one 402L-10kV-NEG-208VAC. The charge supplies are wired in series to create a ±10kV bipolar output. The two output lines each include a series resistor to improve regulation and limit output current under fault conditions. The lines are then split to run a cable to each capacitor module. At the capacitor module, the charge cable is connected across a diode that protects the charge supply in the event of a bank pre-fire (when

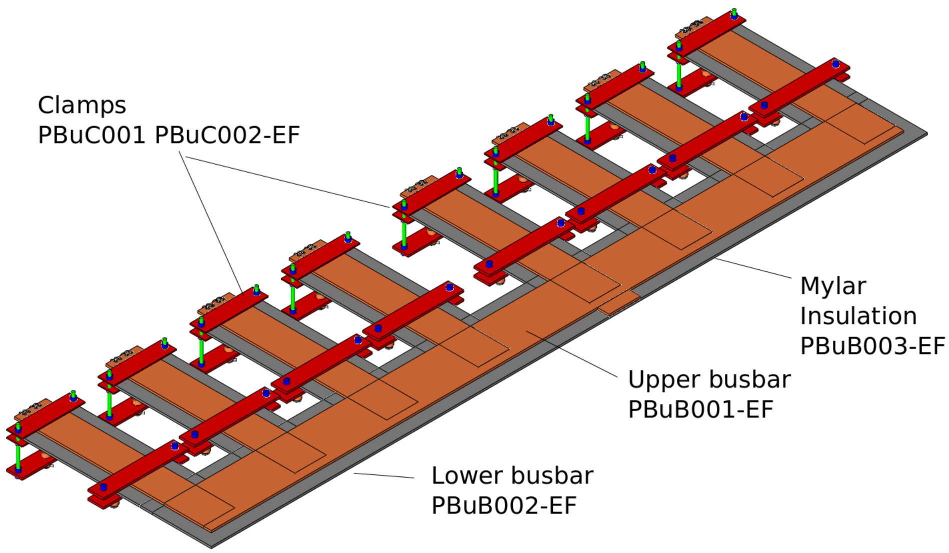


Figure 7: Buswork detail for EF bank.

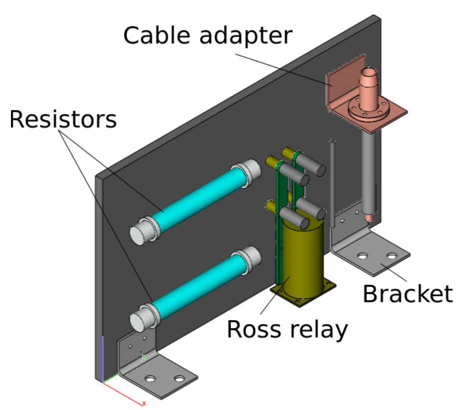


Figure 8: Charging switch and connection detail.

the charge supply is connected to the bank). The diode prevents any bank reversal during pre-fire from imposing a reverse voltage at the charge supply. After the diode is a resistor that limits the charge current for the bank (and limits the protection diode current under reversal). The final connection to the capacitor busswork is made via a normally-open DPST Ross relay (E40-2PNO) which is only connected for charging, and is disconnected immediately prior to programmed discharge. Please refer to the separate specification for the charging supplies (treated as a separate sub-assembly). Charging cable is terminated at the bank with a custom connector, see Fig. 8.

1.8 Dump

Each capacitor module includes a resistor sized to dissipate the full-charge energy of the bank. The resistor material is an aqueous solution of copper sulfate with brass electrodes in a polycarbonate reservoir. The electrolyte concentration is tuned to discharge the bank to below 50 volts (the NFPA 70E safety threshold) within 30 seconds. This dump rate was chosen based upon a conservative estimate of the time required from removal of the Kirk key at the operator station to entry of the bank enclosure. The dump sizing is also designed to allow several sequential full-energy dumps at 3 minute intervals, but in this operation mode the resistor temperature shall be monitored remotely by the operator to ensure the temperature does not

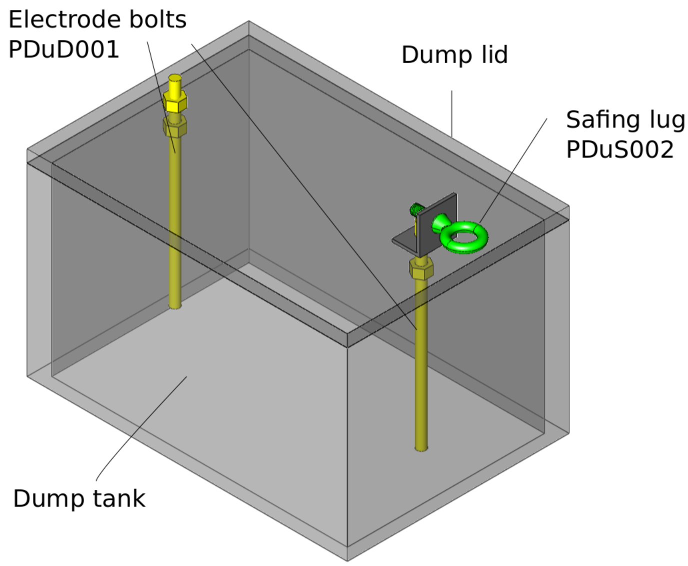


Figure 9: Dump detail for the EF bank module.

exceed 60°C (as per ASTM C1055) and that the water level is maintained. The normally-closed dump relay on each module (Ross E40-NC) will be energized only during charge, and will be de-energized to engage the dump upon removal of the Kirk key or at any emergency stop or interlock break. A temperature sensor is located on the outside lower section of each dump.

1.9 Harnessing

The harnessing sub-assembly comprises all of the interconnecting power cables from the CCDPS to the FLARE machine. The cabling will be triax of suitable current rating (see e.g. Dielectric Sciences specification in the Appendix). 5 cables will connect to the cable header located close to the switches and between the dumps. Cable trays will be used to route cables from the capacitor banks to the device.

1.10 Polarity switching

No polarity switch is required for this module.

1.11 Diagnostics

Diagnostics must be provided to measure the forward current in the bus leading to the forward switch, the voltage of the bank module using a voltage divider, and the temperature of the over-current protection resistor, the temperature in the dump resistor and the temperature at the anode of the ignitrons. Each of these diagnostic measurements must be transmitted along a fiber-optic connection to the DAQ. Please see separate DAQ specifications for further information.

1.12 Safety

Monitoring (analog and digital voltage monitoring) will be required. A voltage divider at the bank will be used to monitor the charging voltage on the control computer (see specification for DAQ), and provide a signal for a panel-mounted analog indicator at the entry to the enclosure. The EF bank module will be housed in a bay that separated it from other bank modules. Each side of the bank module may be separated by a 1/4 inch steel blast shield. The enclosure will be interlocked and procedures will be present to disable the bank before personnel access.

1.13 Cooling requirements

Cooling water is not required for the EF bank modules.

1.14 Connections

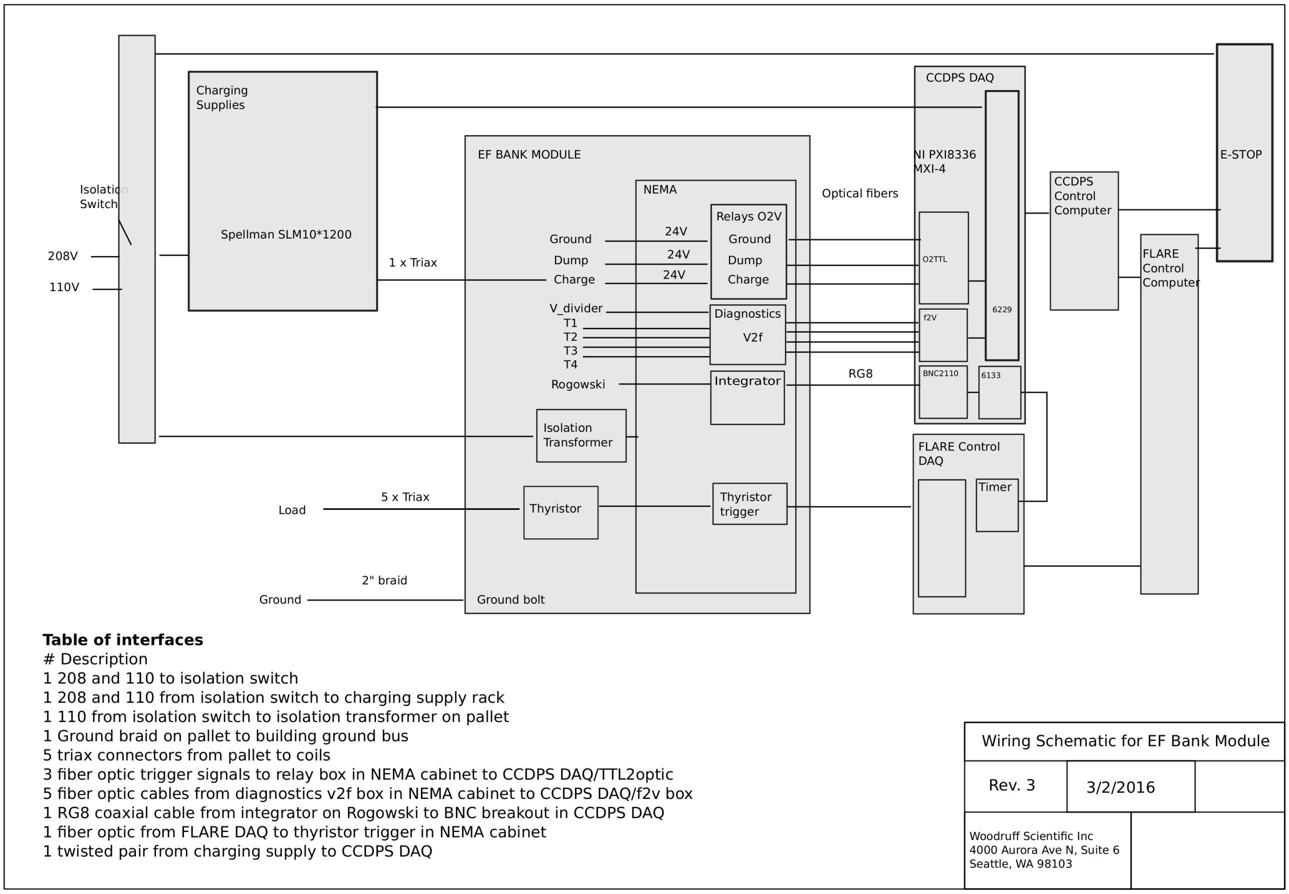


Figure 10: Connections

The connection schematic shows all of the connections that need to be made to the bank modules, power and control systems. From the left of Fig. 10, 208 and 110 power is fed to the bank enclosures via a Kirk key controlled isolation switch. This same switch can be energized by an Emergency Stop (E-stop) button located in the control room (this E-stop is digitized by both the FLARE control DAQ and the CCDPS control DAQ). If energized, the switch will drop all power to the enclosure, thereby killing power to the HV dump (normally closed) and charge (normally open) relays, and dumping bank energy into the cap dumps. The 110 and 208 power is delivered to the charging supply rack (located on it's own separate pallet), and 110 is also delivered to an isolation transformer mounted on the bank module pallet. Connections to the load are made by multiple triax cables (described above). Water is connected to the ignitron switches along 1/4" tubes from a shared chiller unit. The charge, dump ground relays are controlled by individual fiber-optic-enabled switches, with pulse signals sent from the CCDPS DAQ rack (Schematic shown in Fig. 11). Temperature sensor data are transmitted by fiber-optics from the pallet to the DAQ after conversion of voltage to frequency, then reconverting at the DAQ. A BNC connection is made from the current sensor integrator to the DAQ fast data acquisition (sampling at at least 1MHz). Timing synchronization is provided by the FLARE control DAQ. Switch firing is controlled here by the FLARE control computer and DAQ, by transmission of fire signal by fiber-optic connection. CCDPS DAQ requires 110V as input. CCDPS control computer requires 110V as input.

- Electrical input requirements: 208V three phase, 110V, less than 50 Amps (total for all banks at full charge is 100A)
- Load requirements: as specified in [1]
- Cooling requirements: chiller for ignitrons (see specification attached)
- Environmental requirements: dust free, see below
- Control signals needed as inputs: ESTOP and triggers (see Fig. 10)
- Control signals as outputs: none.

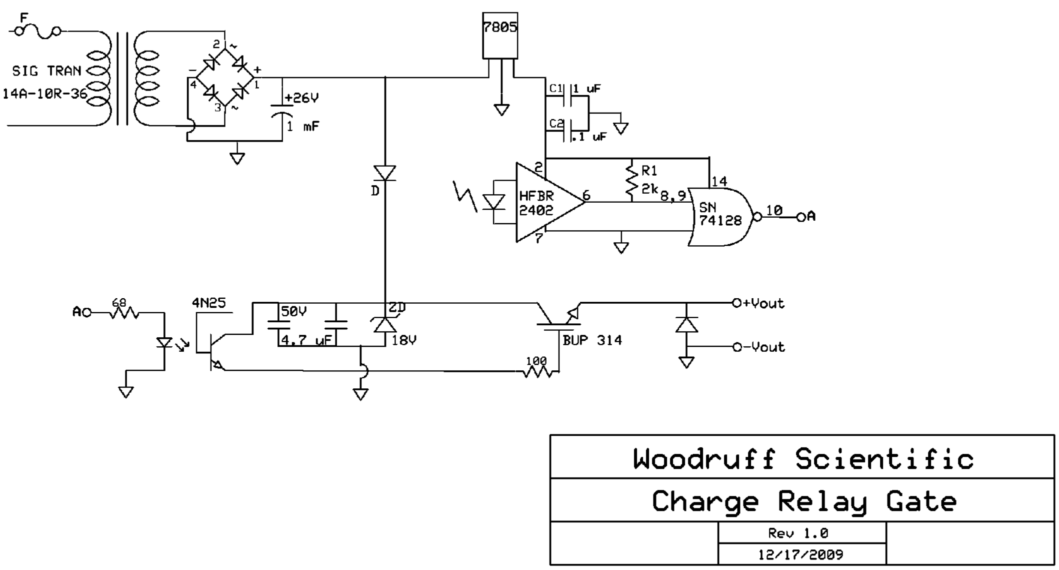


Figure 11: Schematic for charge, dump and ground relay control.

1.15 Environmental requirements

The entire CCDPS is specified to operate at room temperature, and will tolerate seasonal variations in humidity without the need for any special AC, other than cooling lines to the ignitrons. Ideally the banks will be placed in a dust-controlled environment (fans with filters, preferably with drywall to the ceiling), with minimal traffic to the enclosure.

2 References

References

[1] Statement of Work for Design of Capacitor Charge/Discharge Power Supply (CCDPS) for FLARE FLARE-CCDPS-150828, Revision 0, Sept. 9th 2015

3 Appendices

3.1 Engineering Drawings

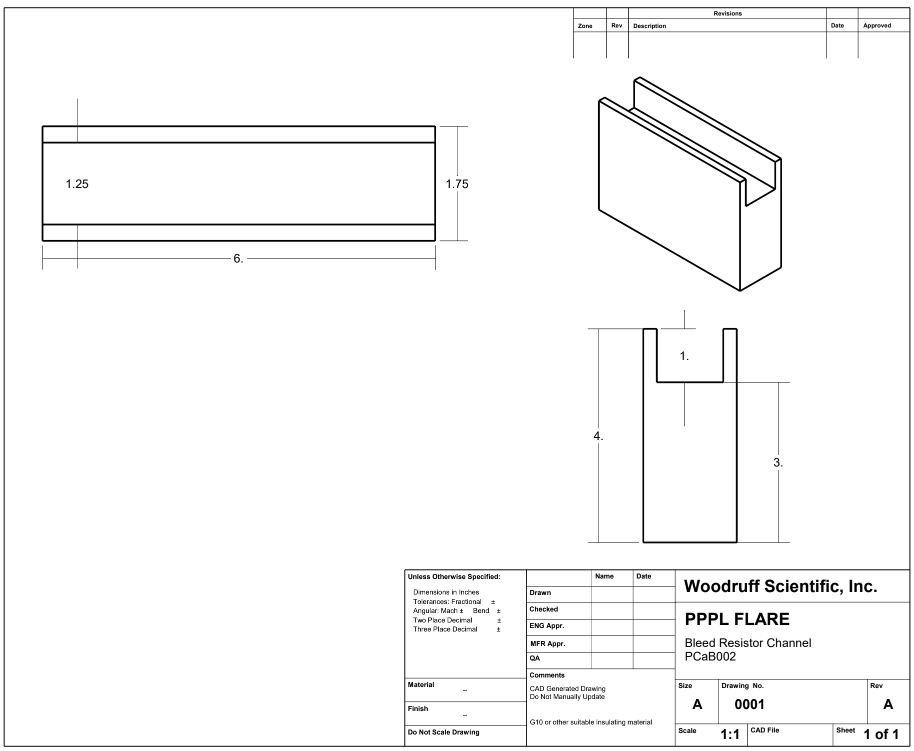


Figure 12: EF Bleed Resistor Channel

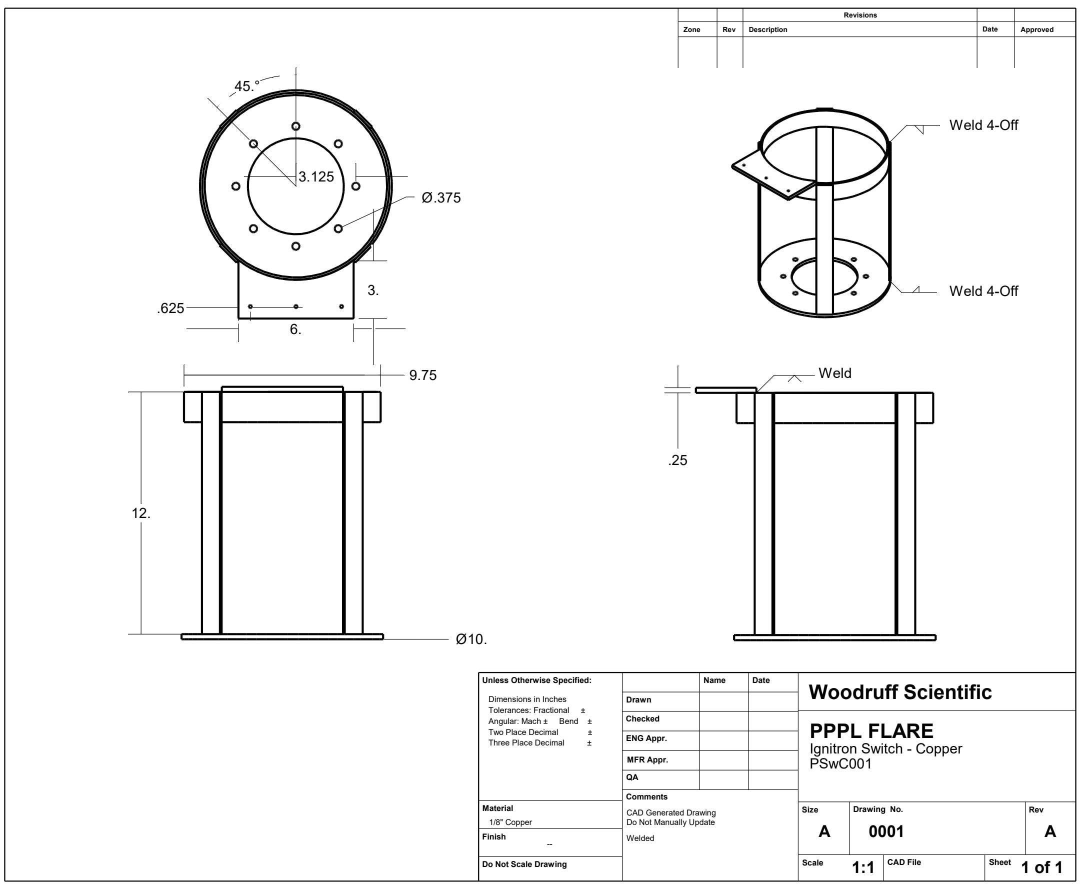


Figure 13: Ignitron Cage - Copper

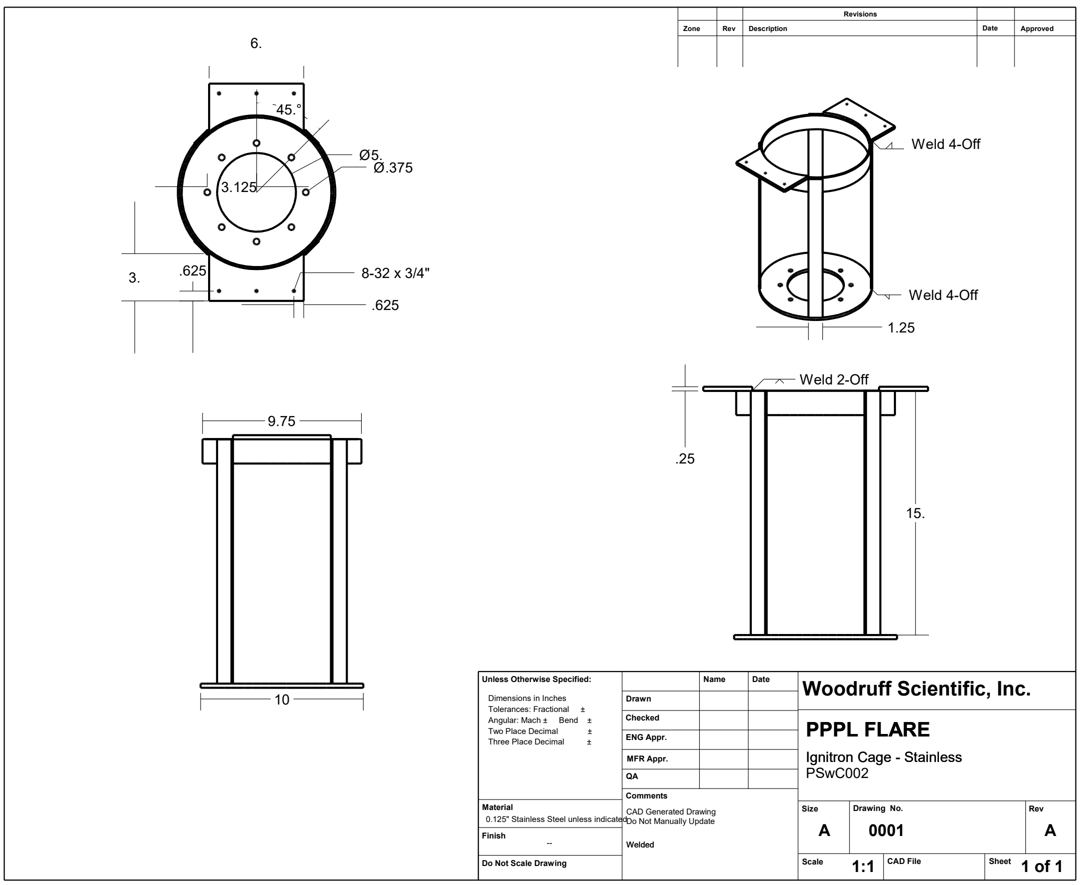


Figure 14: Ignitron Cage - Stainless

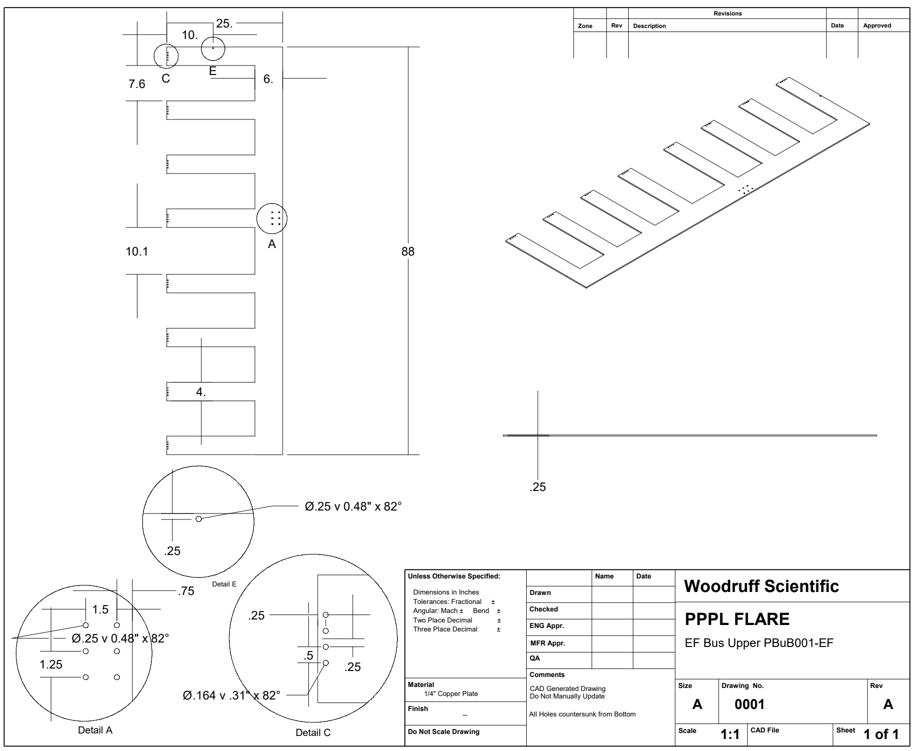


Figure 15: EF Bus Upper

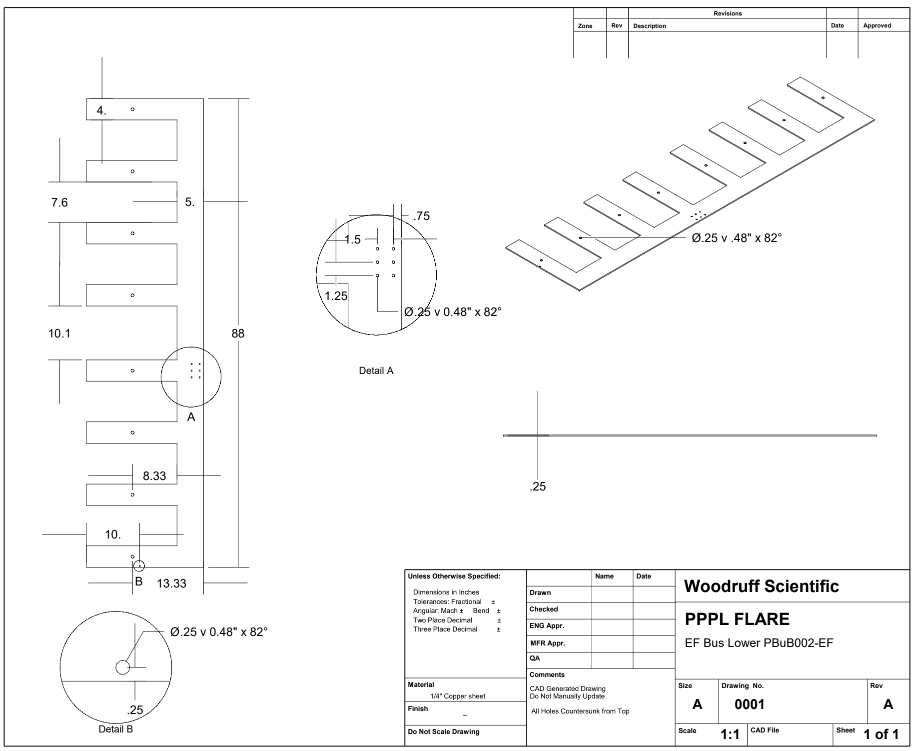


Figure 16: EF Bus Lower

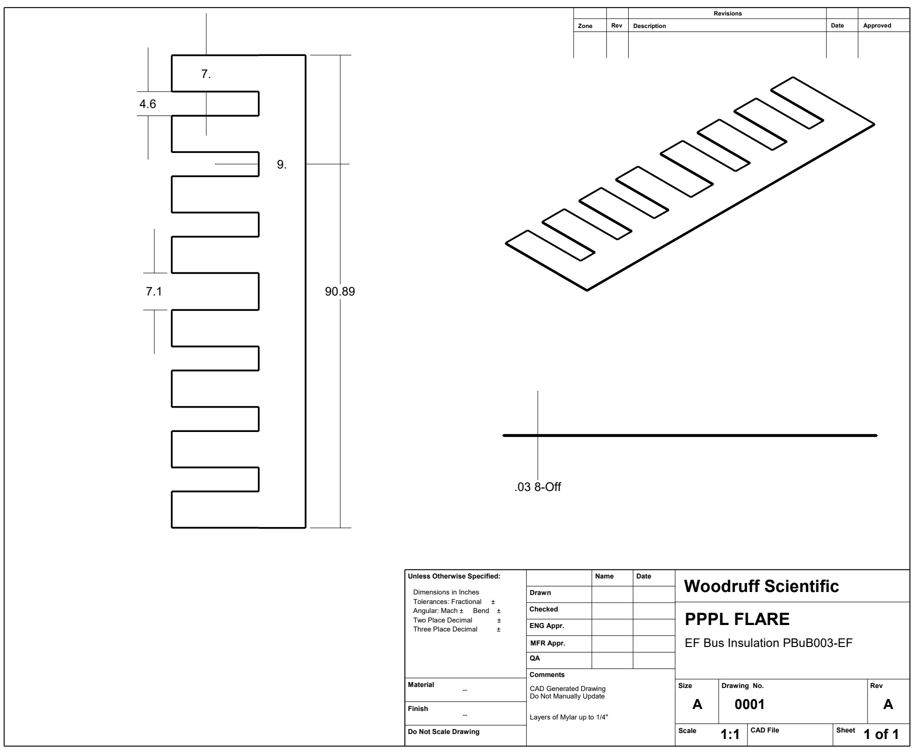


Figure 17: EF Bus Insulation

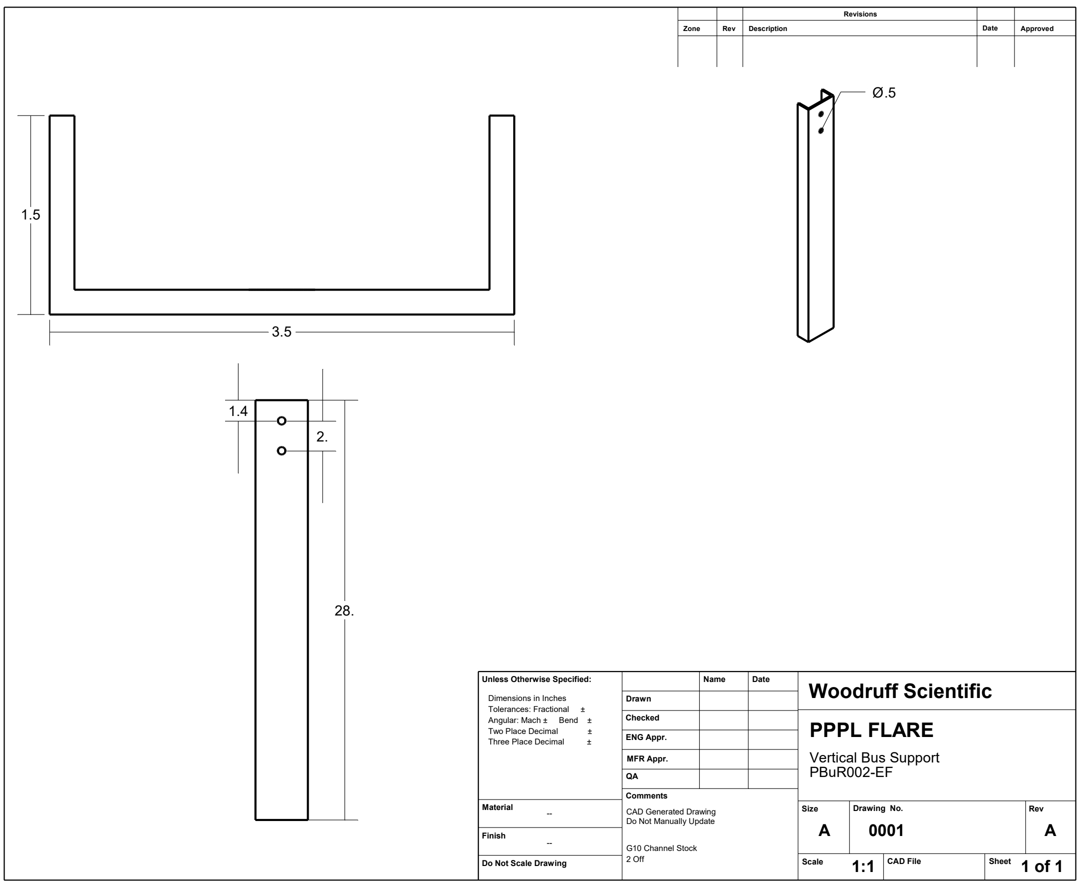


Figure 18: EF Bus Vertical Support - 2 Off

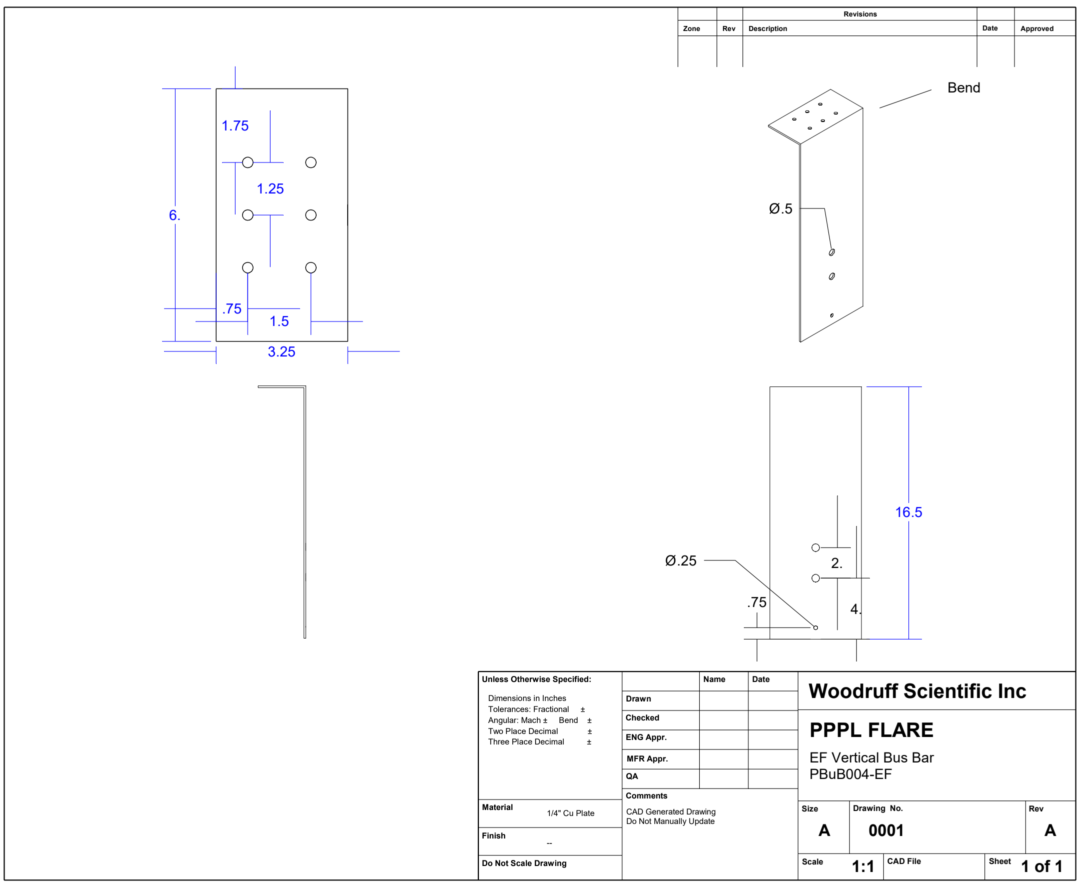


Figure 19: EF Bus Vertical

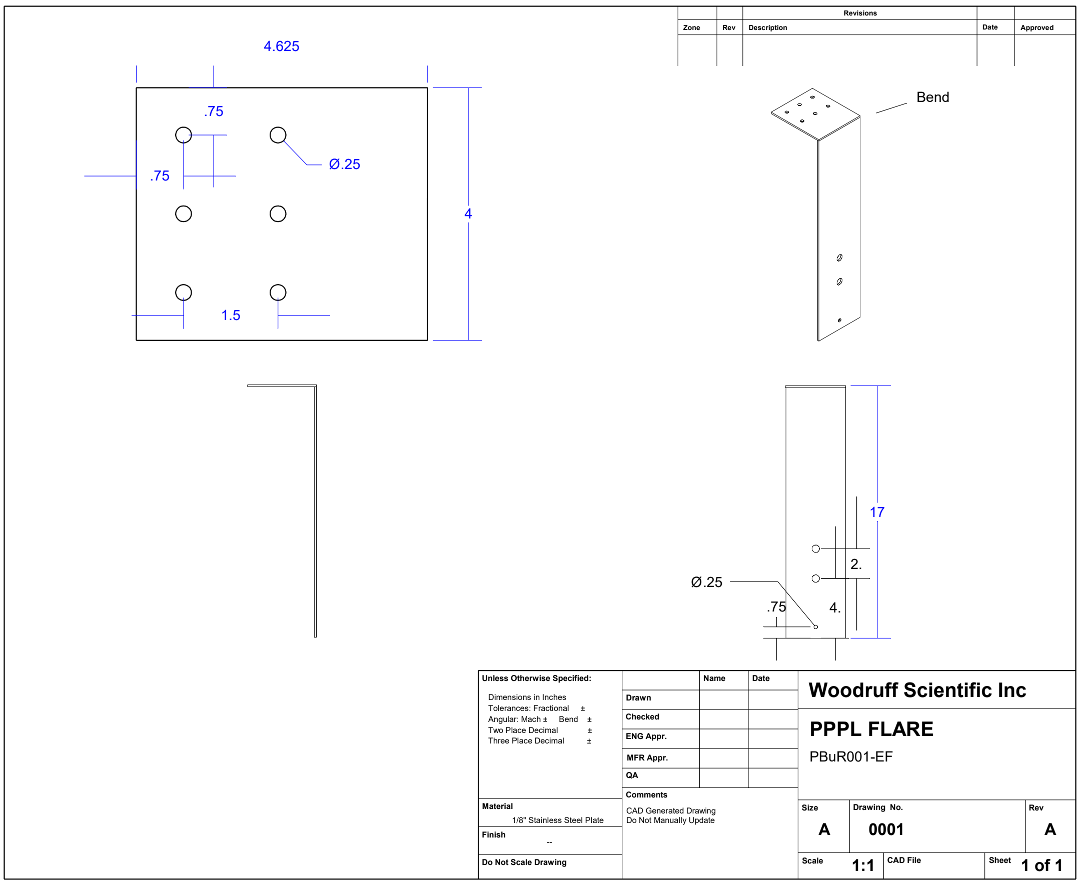


Figure 20: EF Bus Resistor

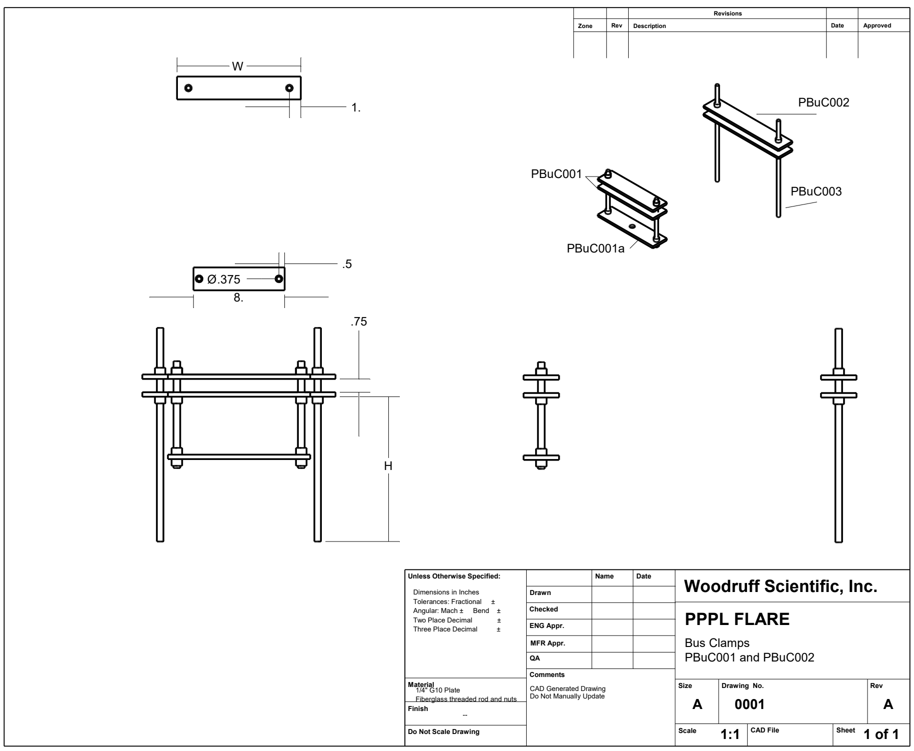


Figure 21: EF Bus Clamps

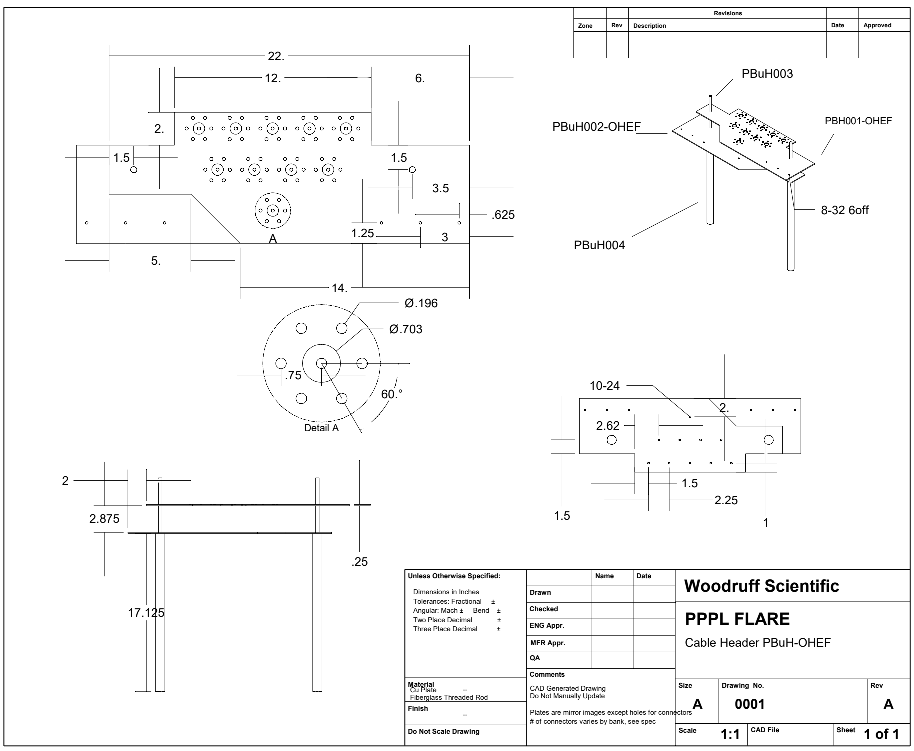


Figure 22: EF Cable Header

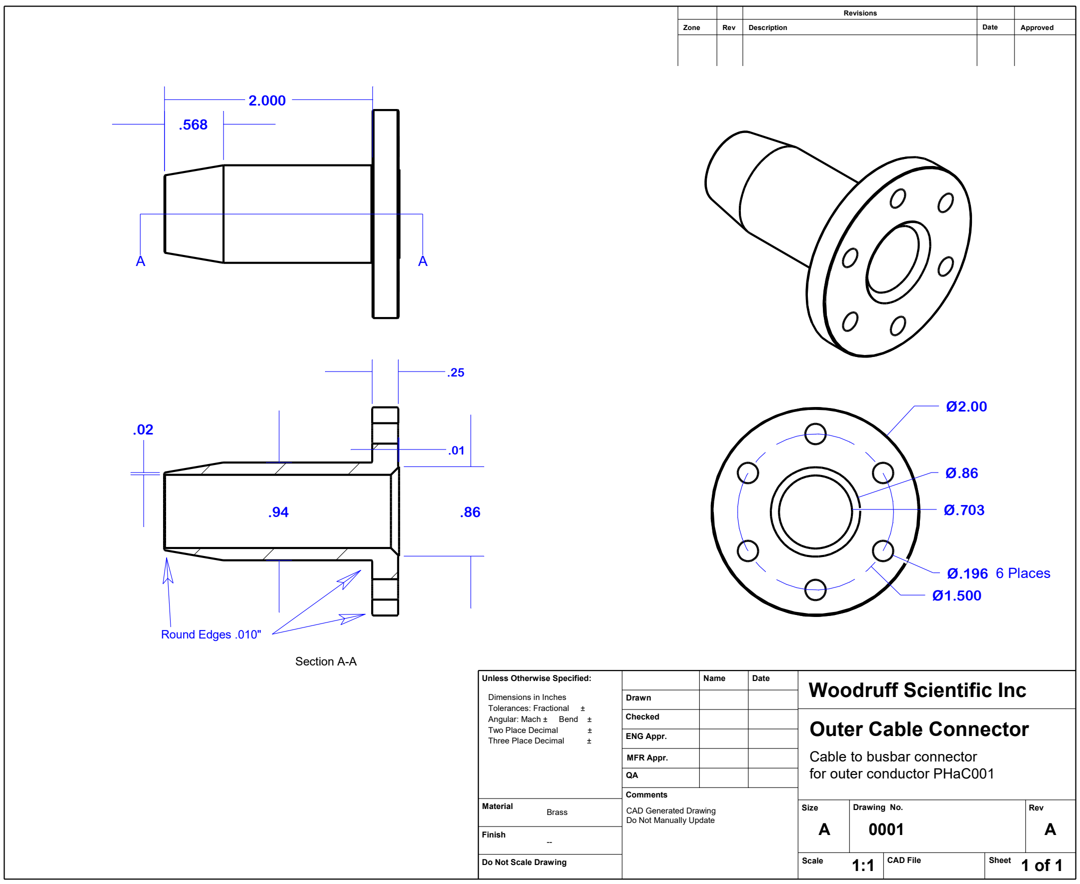


Figure 23: Outer Triax Connector

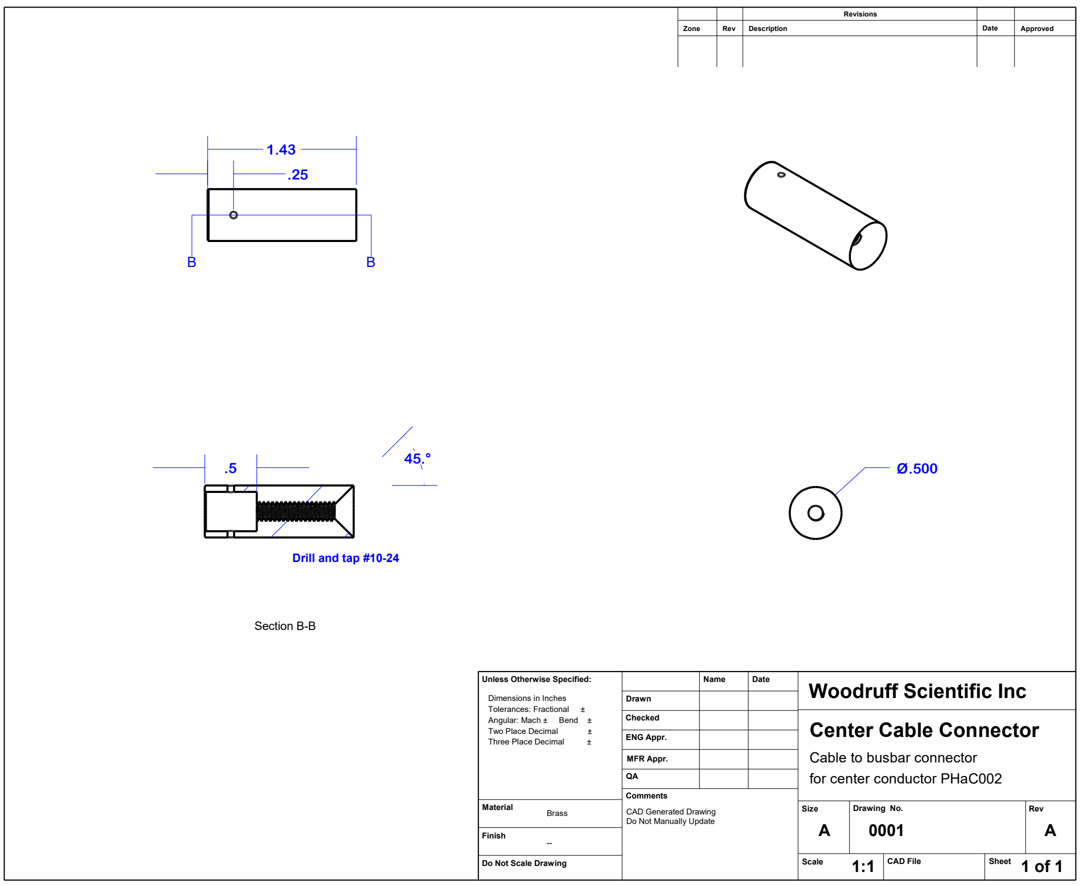


Figure 24: Inner Triax Connector

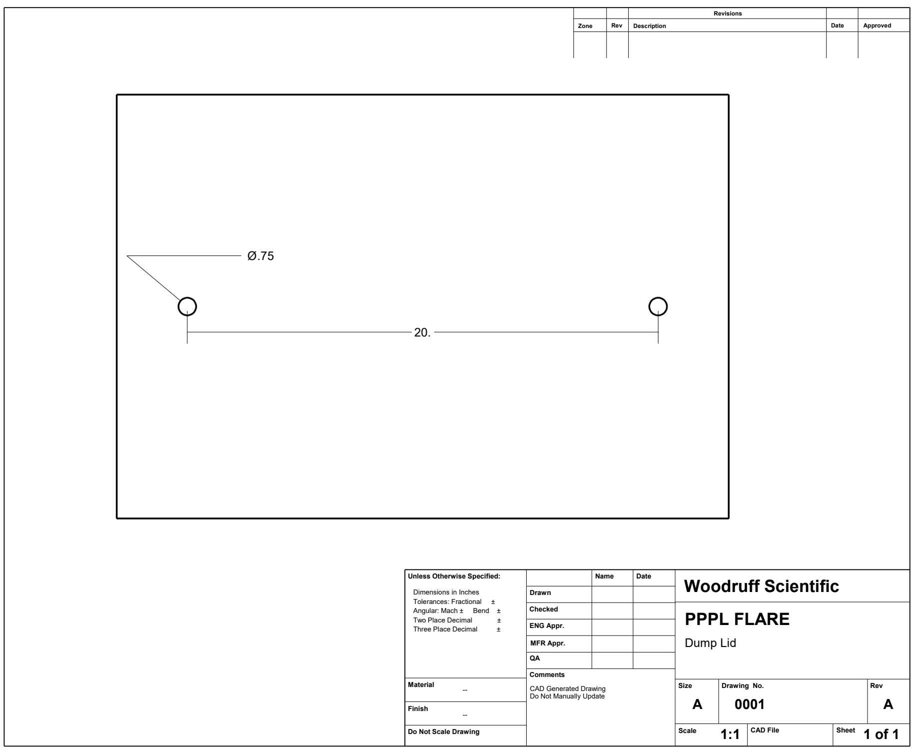


Figure 25: Dump Lid

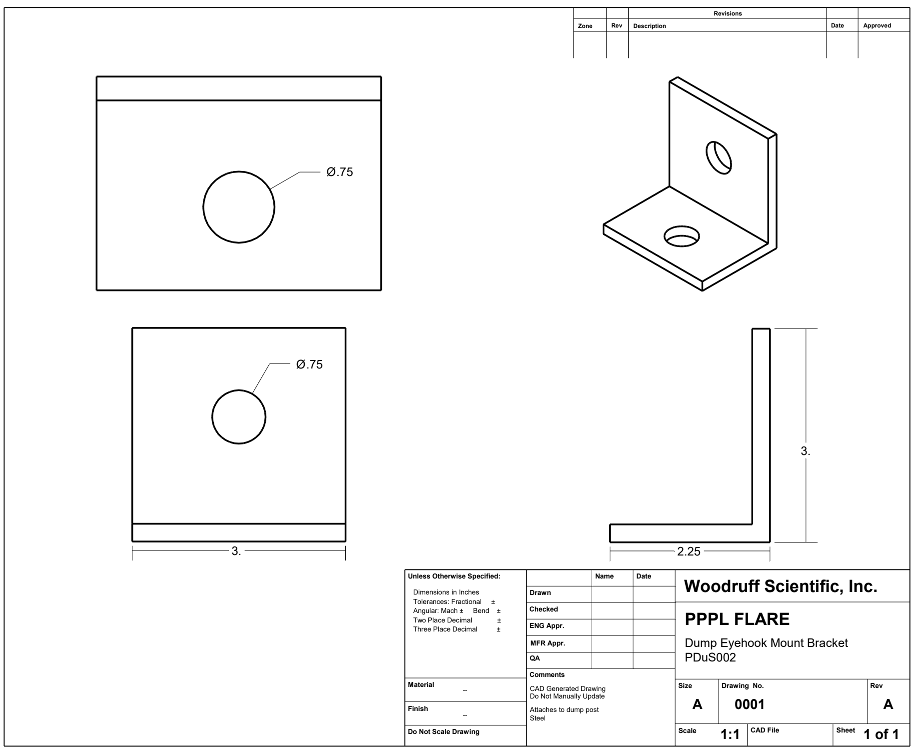


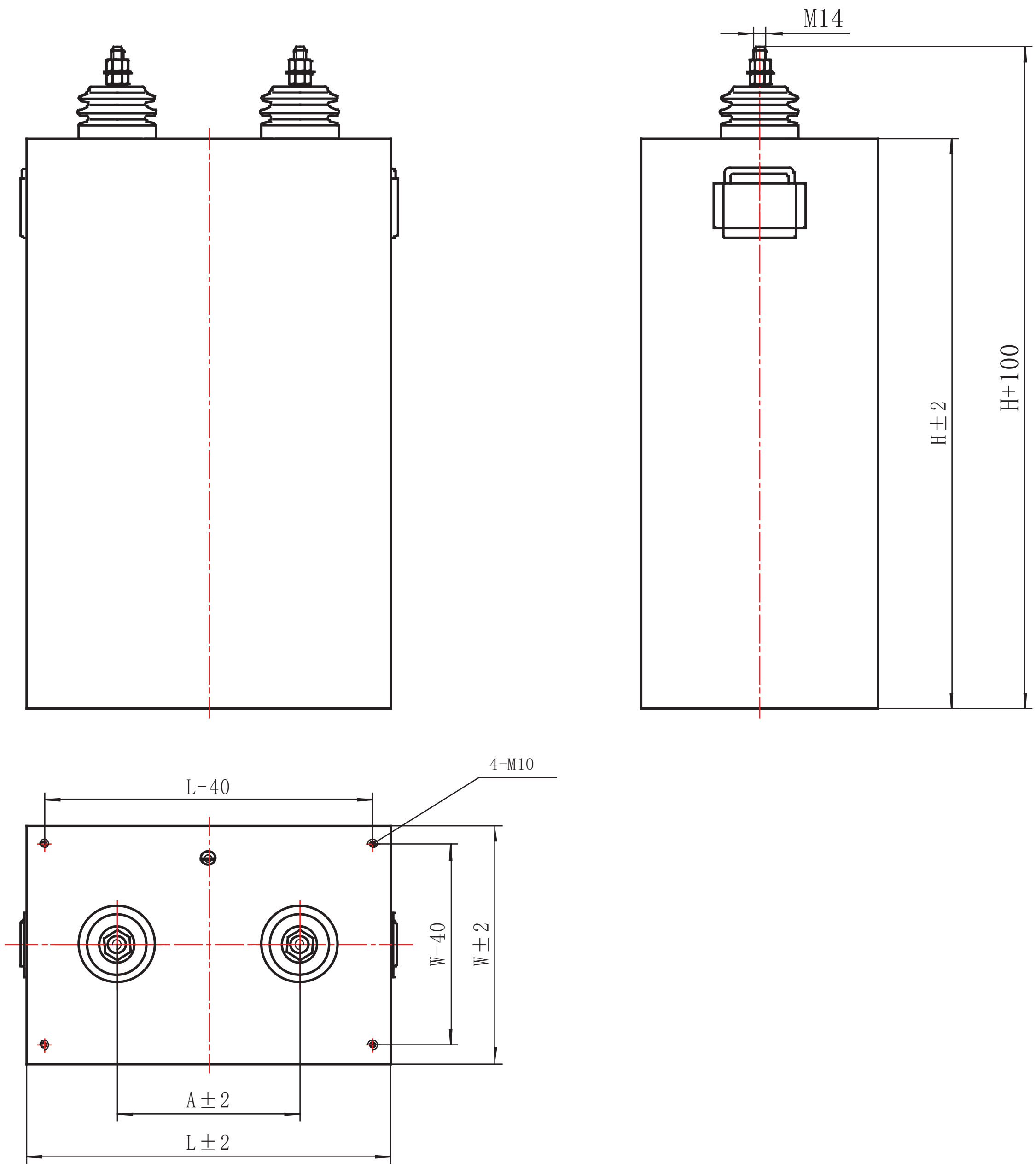
Figure 26: Dump Stick Eyehook Bracket

HDCT 1.4kV 55.65mF Pulse Capacitor

Type		HDCT
Rated voltage	U_{NDC}	1.4kVDC
Rated capacitance	C_N	55650µF
Capacitance tolerance		±5.0%
Rated Discharge Current	I_p	5kA
Max Discharge Current (system fault)	Î	10kA
Rated Discharge Voltage Reversal	%	80%
Self inductance	L_S	< 150 nH
Int. series resistance	R_S	< 5mΩ
Loss factor	tanδ	$< 1.0 \times 10^{-3}$ / 100 Hz
Life Expectancy (90 % survival)		500,000 discharges
Operating temperature	Θmin/ max	-40°C / +70 °C
Technology		Metalized Polypropylene film, dry type, SH
Dimensions(mm^3)		420×270×645

NL55650-1.4KVDC

HIGH DENSITY CHARGE TRANSFER CAPACITOR



Specification	L（mm）	W（mm）	H（mm）	A（mm）
1.4kV 55650μF	420	270	645	220

V_{RSM}	=	4000	V
$I_{F(AV)M}$	=	5200	A
$I_{F(RMS)}$	=	8200	A
I_{FSM}	=	85×10^3	A
V_{F0}	=	0.8	V
r_F	=	0.086	mΩ

Rectifier Diode
5SDD 54N4000

Doc. No. 5SYA1171-00 Dec. 03

- **Patented free-floating silicon technology**
- **Very low on-state losses**
- **Optimum power handling capability**

Blocking

Maximum rated values [1)]

Parameter	Symbol	Conditions	Value	Unit
Repetitive peak reverse voltage	V_{RRM}	f = 50 Hz, t_p = 10ms, T_j = 0...150°C	3600	V
Non - repetitive peak reverse voltage	V_{RSM}	f = 5 Hz, t_p = 10ms, T_j = 0...150°C	4000	V

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. (reverse) leakage current	I_{RRM}	V_{RRM}, Tj = 150°C			400	mA

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		81	90	108	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				2.8	kg
Housing thickness	H	F_M = 90 kN, T_a = 25 °C			35.9	mm
Surface creepage distance	D_S		56			mm
Air strike distance	D_a		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Max. average on-state current	$I_{F(AV)M}$	50 Hz, Half sine wave, T_C = 85 °C			5200	A
Max. RMS on-state current	$I_{F(RMS)}$				8200	A
Max. peak non-repetitive surge current	I_{FSM}	t_p = 10 ms, T_j = 150°C, V_R = 0 V			85×10^3	A
Limiting load integral	I^2t				36.3×10^6	A^2s
Max. peak non-repetitive surge current	I_{FSM}	t_p = 8.3 ms, T_j = 150°C, V_R = 0 V			90×10^3	A
Limiting load integral	I^2t				34.6×10^6	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_F	I_F = 5000 A, T_j = 150°C			1.23	V
Threshold voltage	$V_{(T0)}$	T_j = 150°C I_T = 2500...7500 A			0.8	V
Slope resistance	r_T				0.086	mΩ

Switching

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	di_F/dt = -10 A/µs, V_R = 200 V I_{FRM} = 4000 A, T_j = 150°C			18000	µAs

Thermal

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}		0		150	°C
Storage temperature range	T_{stg}		-40		150	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 81...108 kN			5.7	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 81...108 kN			11.4	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 81...108 kN			11.4	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 81...108 kN			1	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 81...108 kN			2	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th\,i}\left(1 - e^{-t/\tau_i}\right)$$

i	1	2	3	4
$R_{th\,i}$(K/kW)	3.728	1.248	0.433	0.292
τ_i(s)	0.8115	0.1014	0.0089	0.0015

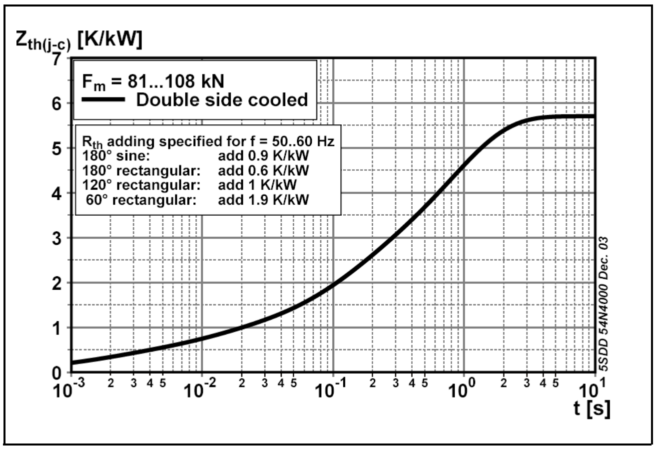


Fig. 1 Transient thermal impedance junction-to-case.

Max. on-state characteristic model:

$$V_{F25} = A_{Tvj} + B_{Tvj} \cdot I_F + C_{Tvj} \cdot \ln(I_F + 1) + D_{Tvj} \cdot \sqrt{I_F}$$

Valid for I_F = 300 – 110000 A

A_{25}	B_{25}	C_{25}	D_{25}
486.40×10^{-3}	45.53×10^{-6}	65.82×10^{-3}	68.19×10^{-15}

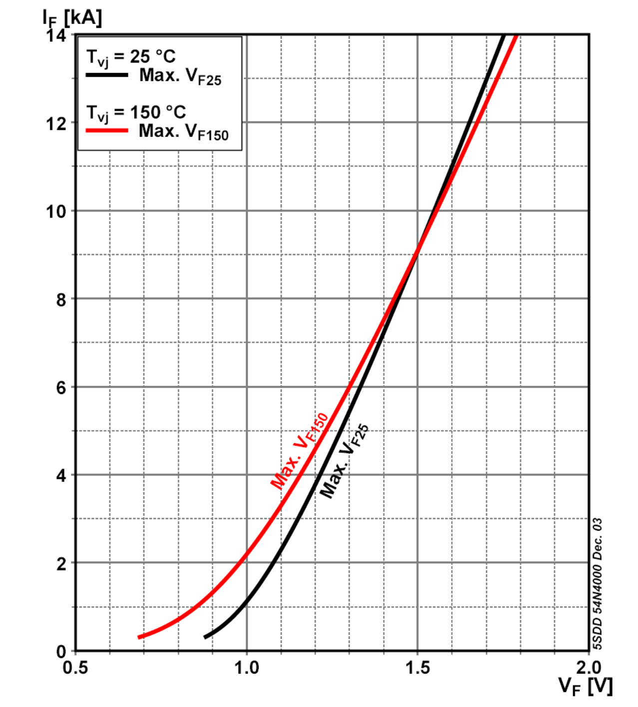


Fig. 2 Isothermal on-state characteristics

Max. on-state characteristic model:

$$V_{F150} = A_{Tvj} + B_{Tvj} \cdot I_F + C_{Tvj} \cdot \ln(I_F + 1) + D_{Tvj} \cdot \sqrt{I_F}$$

Valid for I_F = 300 – 110000 A

A_{150}	B_{150}	C_{150}	D_{150}
22.00×10^{-3}	49.09×10^{-6}	113.10×10^{-3}	-20.75×10^{-15}

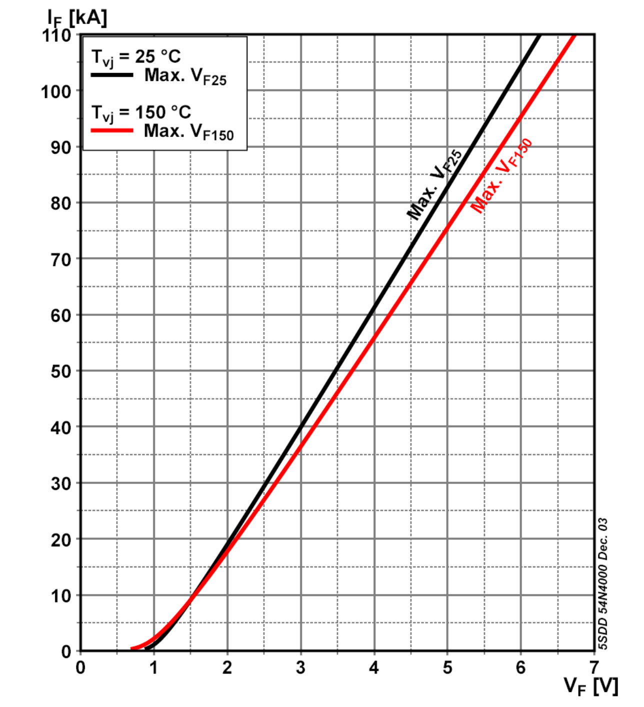


Fig. 3 Isothermal on-state characteristics

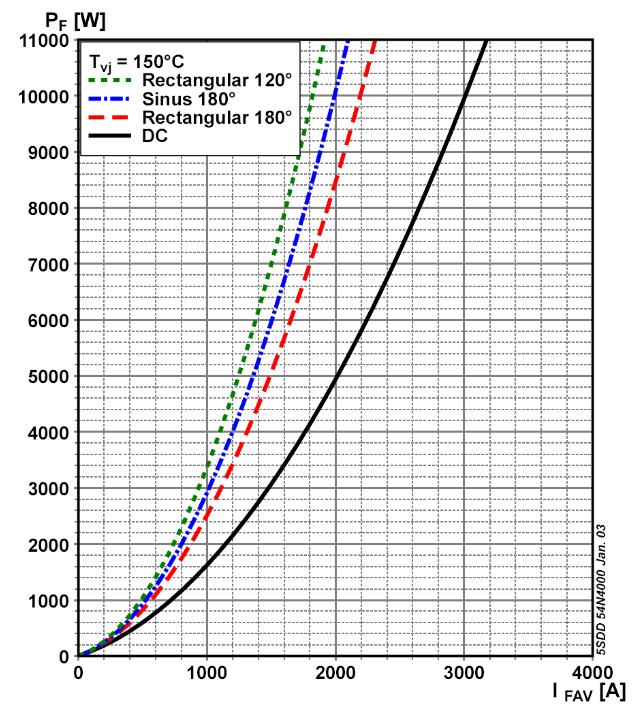


Fig. 4 On-state power losses vs average on-state current.

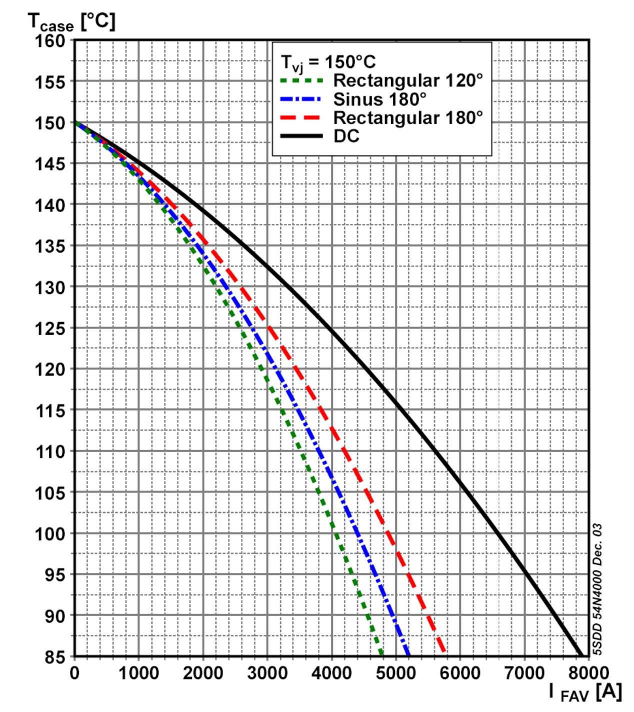


Fig. 5 Max. permissible case temperature vs average on-state current.

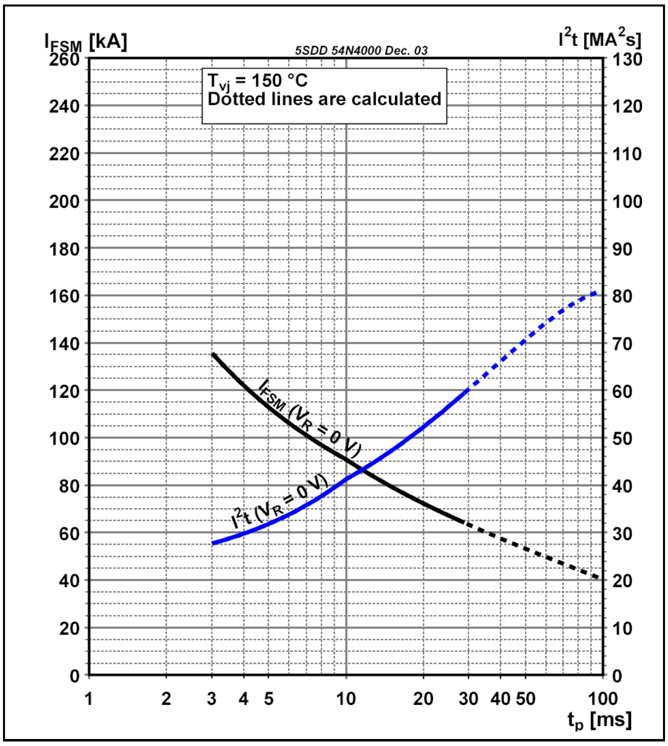


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

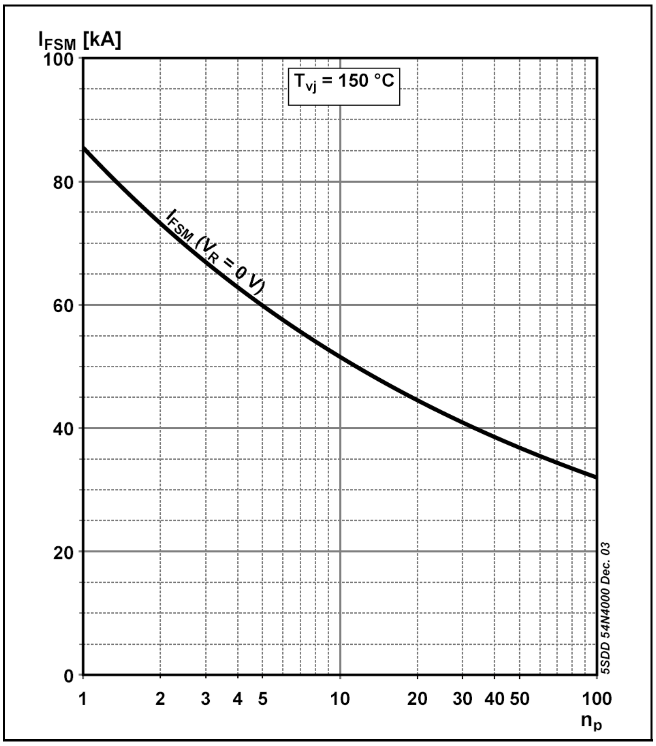


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

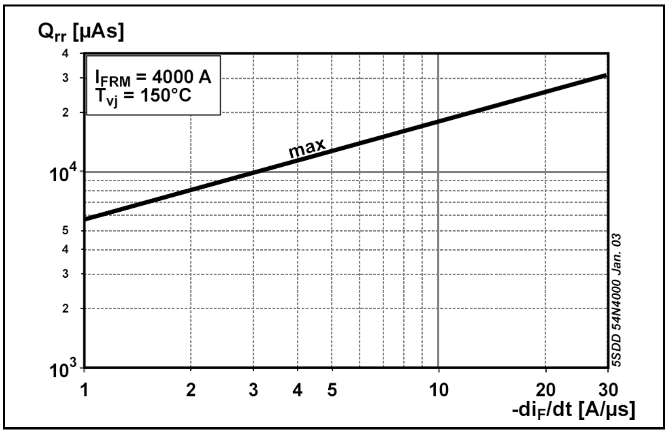


Fig. 8 Recovery charge vs. decay rate of on-state current.

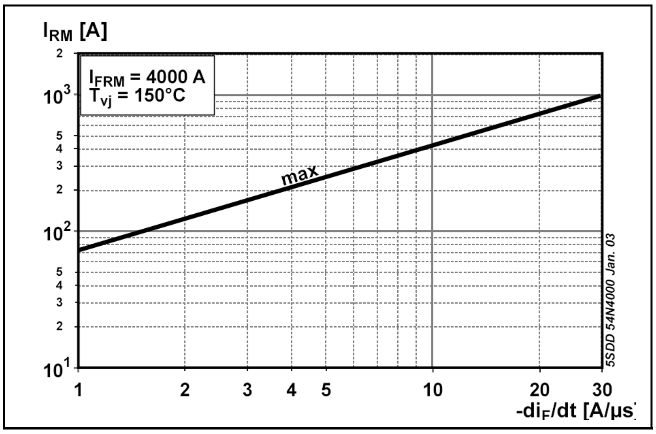


Fig. 9 Peak reverse recovery current vs. decay rate of on-state current.

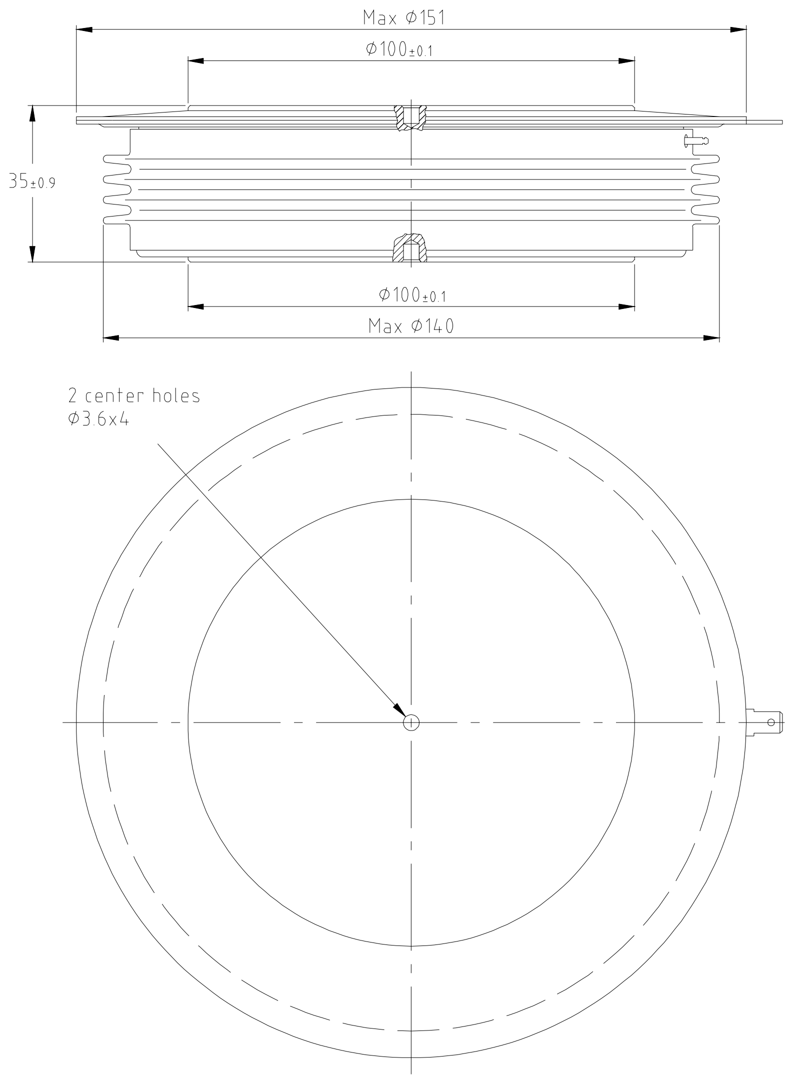


Fig. 10 Outline drawing. All dimensions are in millimeters and represent nominal values unless stated otherwise.

Related application notes:

Doc. Nr	Titel
5SYA 2020	Design of RC-Snubbers for Phase Control Applications
5SYA 2029	Designing Large Rectifiers with High Power Diodes
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors

Please refer to http://www.abb.com/semiconductors for actual versions.

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Doc. No. 5SYA1171-00 Dec. 03

V_{DRM}	=	1800 V
$I_{T(AV)M}$	=	6100 A
$I_{T(RMS)}$	=	9600 A
I_{TSM}	=	$94.0 \cdot 10^3$ A
V_{T0}	=	0.9 V
r_T	=	0.05 mΩ

Phase Control Thyristor

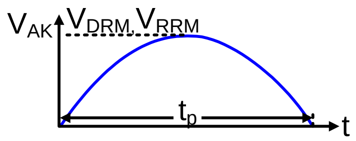
5STP 50Q1800

Doc. No. 5SYA1070-02 Mar. 14

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

Blocking

Maximum rated values ***1)***

Parameter	Symbol	Conditions	5STP 50Q1800	Unit
Max repetitive peak forward and reverse blocking voltage	V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms, T_{vj} = 5…125 °C, Note 1 	1800	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to $0.67 \cdot V_{DRM}$, T_{vj} = 125 °C	1000	V/µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	V_{DRM}, T_{vj} = 125 °C			300	mA
Reverse leakage current	I_{RRM}	V_{RRM}, T_{vj} = 125 °C			300	mA

Note 1: Voltage de-rating factor of 0.11% per °C is applicable for T_{vj} below +5 °C.

Mechanical data

Maximum rated values ***1)***

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		81	90	108	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				2.1	kg
Housing thickness	H	F_M = 90 kN, T_a = 25 °C	25.5		26.5	mm
Surface creepage distance	D_s		36			mm
Air strike distance	D_a		15			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

ABB Switzerland Ltd, Semiconductors reserves the right to change specifications without notice.

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, Tc = 70 °C			6100	A
RMS on-state current	$I_{T(RMS)}$				9600	A
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, V_D = V_R= 0 V, after surge			$94.0 \cdot 10^3$	A
Limiting load integral	I^2t				$44.18 \cdot 10^6$	A^2s
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, V_R = 0.6·V_{RRM}, after surge			$88.0 \cdot 10^3$	A
Limiting load integral	I^2t				$38.72 \cdot 10^6$	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 3000 A, T_{vj} = 125 °C			1.04	V
Threshold voltage	$V_{(T0)}$	I_T = 4000 A - 18000 A, T_{vj} = 125 °C			0.9	V
Slope resistance	r_T				0.05	mΩ
Holding current	I_H	T_{vj} = 25 °C			100	mA
		T_{vj} = 125 °C			75	mA
Latching current	I_L	T_{vj} = 25 °C			500	mA
		T_{vj} = 125 °C			350	mA

Switching

Maximum rated values [1)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_{vj} = 125 °C, I_{TRM} = 3000 A, $V_D \leq 0.67 \cdot V_{DRM}$, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 50 Hz			250	A/µs
			Cont. f = 1 Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 125 °C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20 V/µs				500	µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	T_{vj} = 125 °C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs	1500		3000	µAs
Reverse recovery current	I_{RM}		45		70	A
Gate turn-on delay time	t_{gd}	T_{vj} = 25 °C, V_D = 0.4·V_{RM}, I_{FG} = 2 A, t_r = 0.5 µs			3	µs

Triggering

***Maximum rated values* [1)]**

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$			see Fig. 7		W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			0.3	V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			10	mA

Thermal

***Maximum rated values* [1)]**

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 81... 108 kN			5	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 81... 108 kN			10	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 81... 108 kN			10	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 81... 108 kN			1	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 81... 108 kN			2	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j\text{-}c)}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/\tau_i}\right)$$

i	1	2	3	4
R_i(K/kW)	3.359	0.936	0.481	0.224
τ_i(s)	0.4069	0.0854	0.0118	0.0030

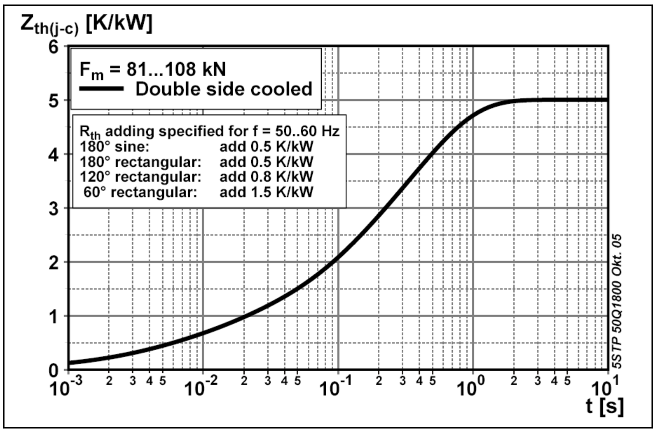


Fig. 1 Transient thermal impedance (junction-to-case) vs. time

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 200 - 100000 A

A_{25}	B_{25}	C_{25}	D_{25}
$932.0 \cdot 10^{-3}$	$25.28 \cdot 10^{-6}$	$-14.74 \cdot 10^{-3}$	$3.721 \cdot 10^{-3}$

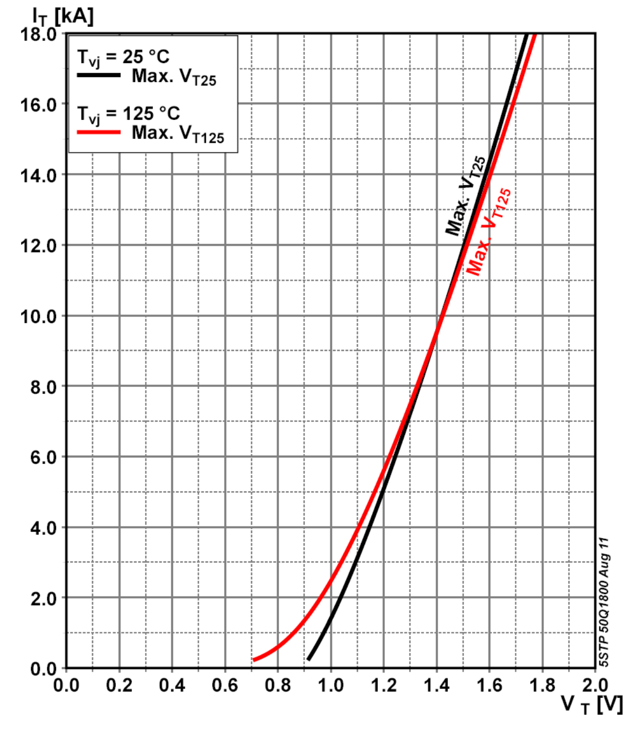


Fig. 2 On-state voltage characteristics

Max. on-state characteristic model:

$$V_{T125} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 200 - 100000 A

A_{125}	B_{125}	C_{125}	D_{125}
$334.7 \cdot 10^{-3}$	$29.36 \cdot 10^{-6}$	$61.2 \cdot 10^{-3}$	$2.313 \cdot 10^{-3}$

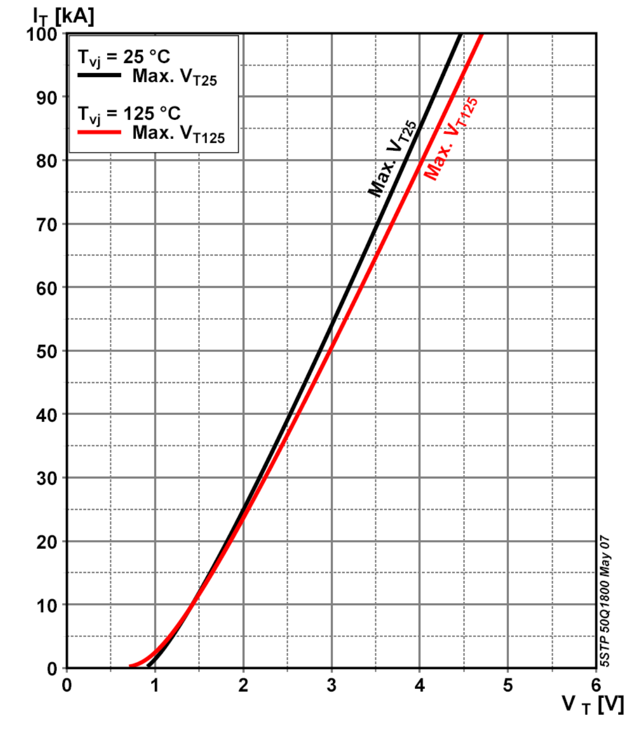


Fig. 3 On-state voltage characteristics

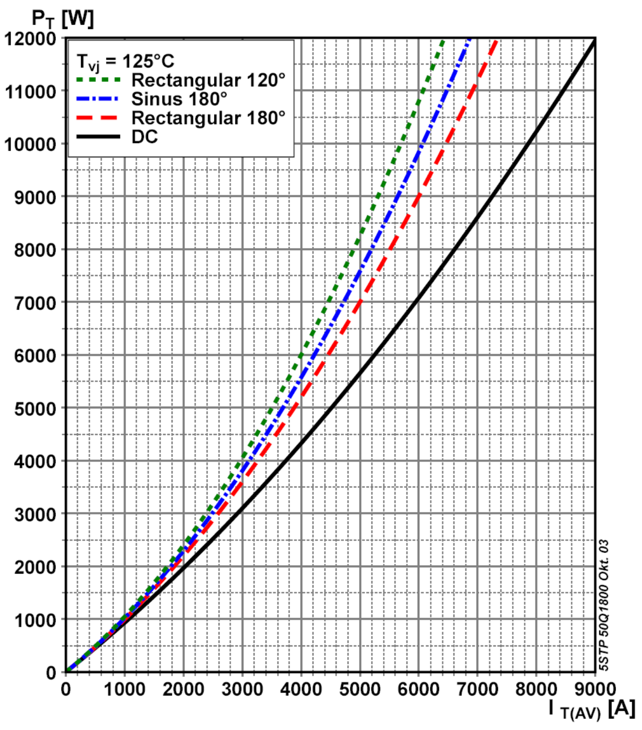


Fig. 4 On-state power dissipation vs. mean on-state current, turn-on losses excluded

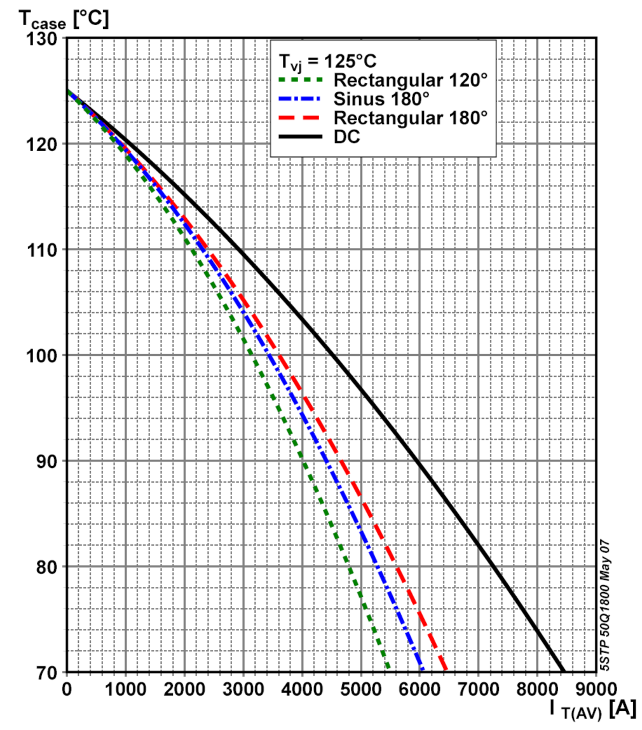


Fig. 5 Max. permissible case temperature vs. mean on-state current, switching losses ignored

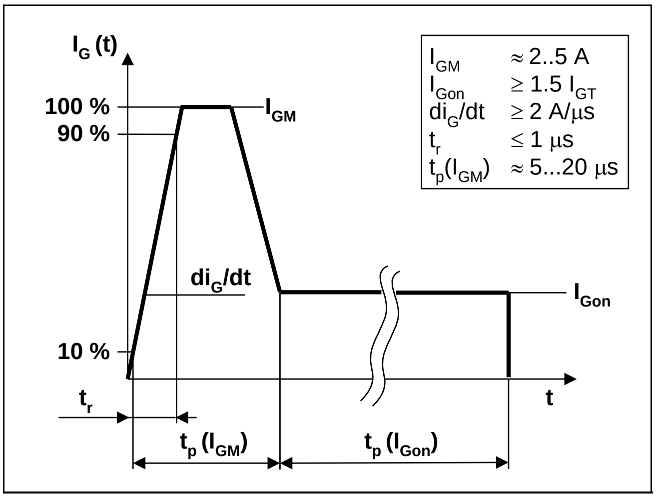


Fig. 6 Recommended gate current waveform

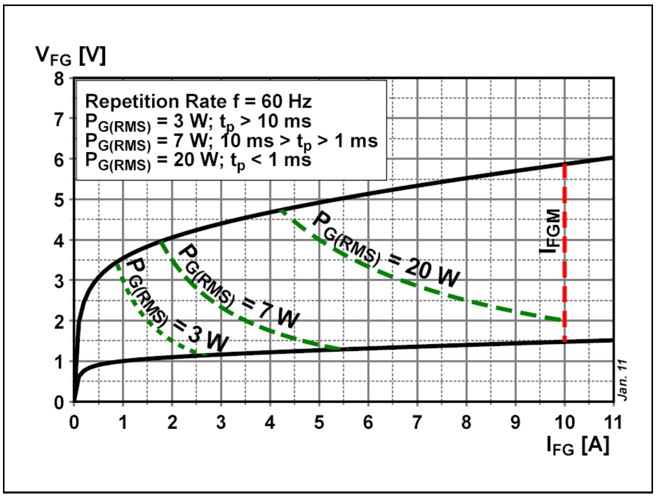


Fig. 7 Max. peak gate power loss

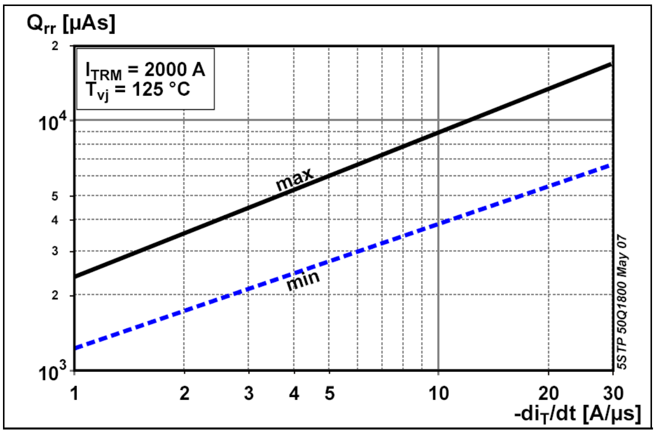


Fig. 8 Reverse recovery charge vs. decay rate of on-state current

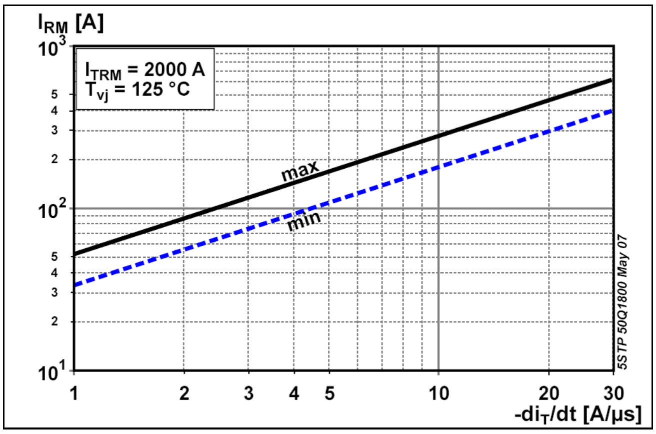


Fig. 9 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

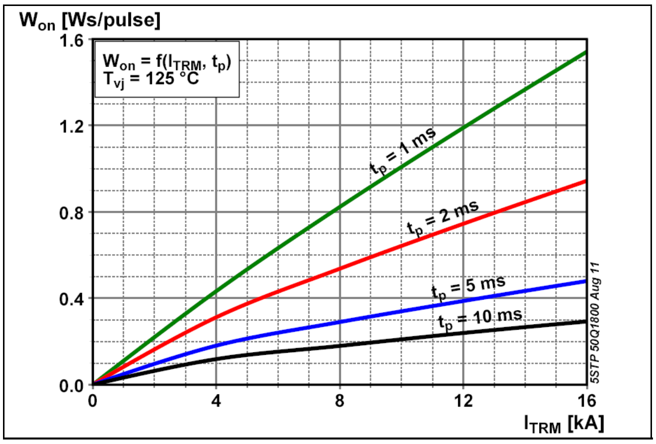


Fig. 10 Turn-on energy, half sinusoidal waves

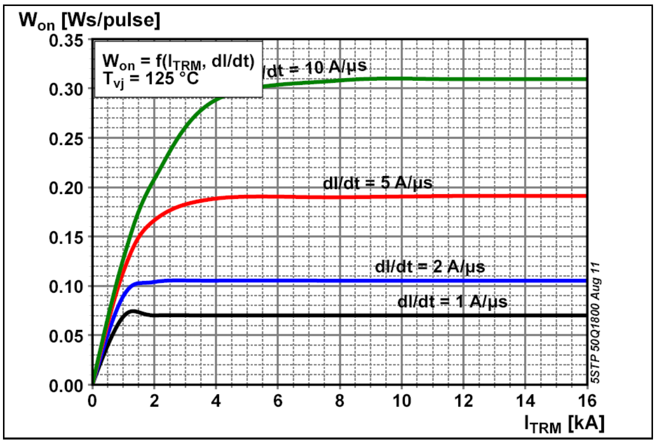


Fig. 11 Turn-on energy, rectangular waves

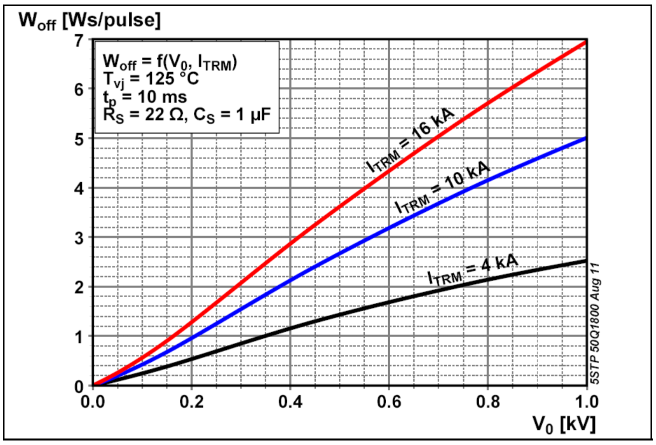


Fig. 12 Turn-off energy, half sinusoidal waves

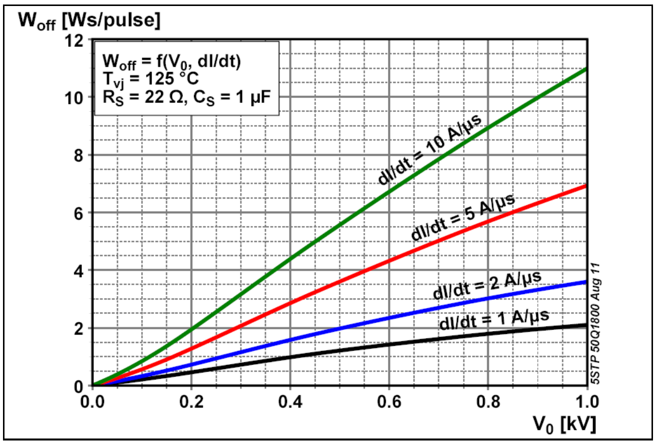


Fig. 13 Turn-off energy, rectangular waves

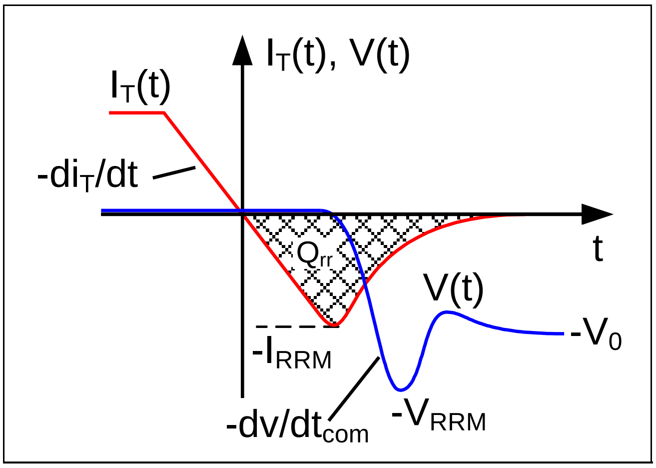


Fig. 14 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T}\int_0^T I_T \cdot V_T(I_T)\ dt$$

Fig. 15 Relationships for power loss

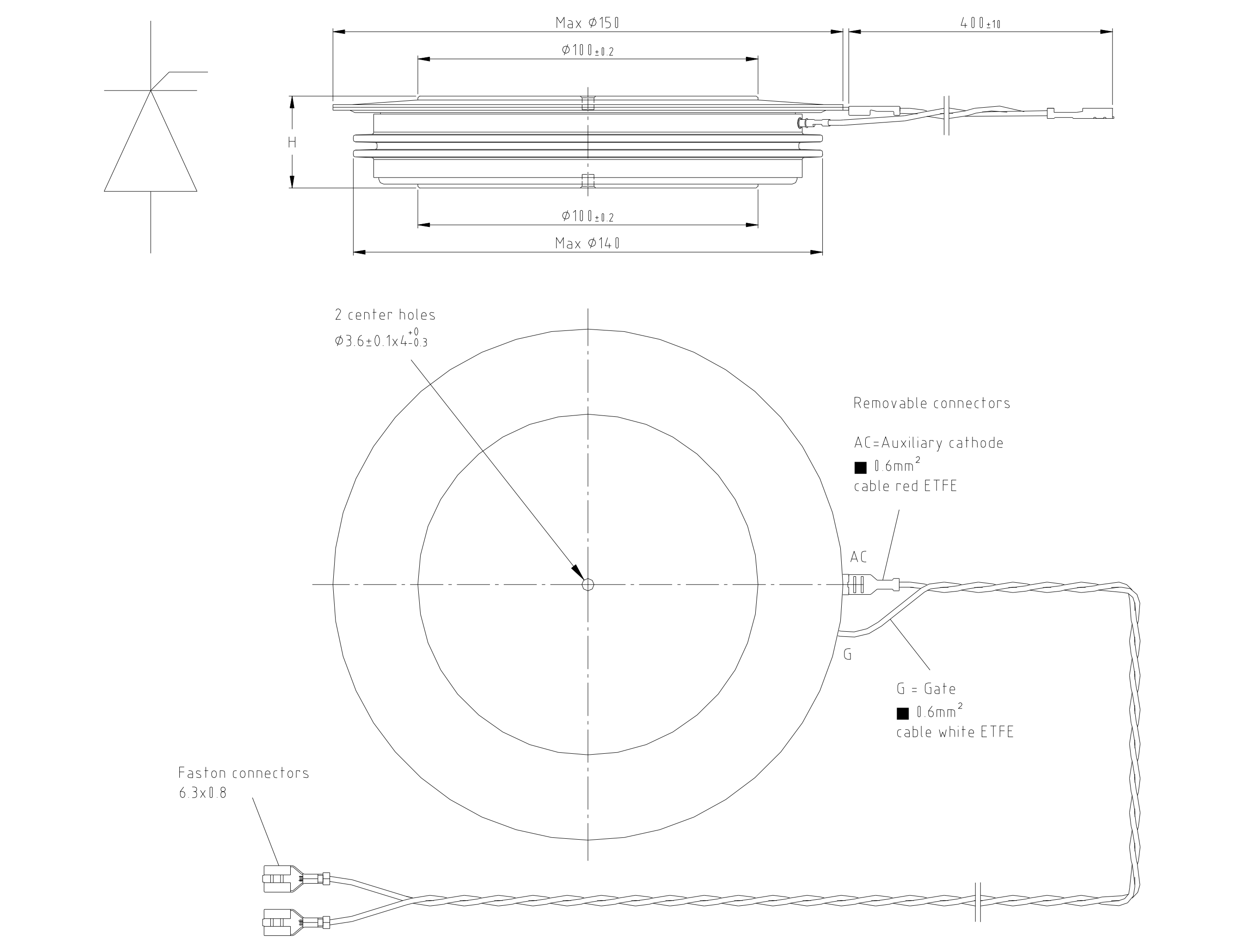


Fig. 16 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubber for Phase Control Applications
5SYA 2049	Voltage definitions for phase control thyristors and diodes
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-Drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
5SYA 2102	Surge currents for Phase Control Thyristors
5SZK 9104	Specification of environmental class for pressure contact diodes, PCTs and GTO, STORAGE
5SZK 9105	Specification of environmental class for pressure contact diodes, PCTs and GTO, TRANSPORTATION
5SZK 9115	Specification of environmental class for presspack Diodes, PCTs and GTOs, OPERATION (Industry)
5SZK 9116	Specification of environmental class for presspack Diodes, PCTs and GTOs, OPERATION (Traction)

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a.l.e. systems

402 Series Data Sheet

High Voltage Power Supply
Capacitor Charging and DC
Output Voltage from 1kV - 50kV
Output Power 4kJ/sec or 4kW
Full local and remote control

TDK·Lambda

www.us.tdk-lambda.com/hp

402 Series Specification

Industry standard rack mount capacitor charging and DC power supplies with 4kJ/sec rating for capacitor charging, or 4kW rating in continuous DC applications.

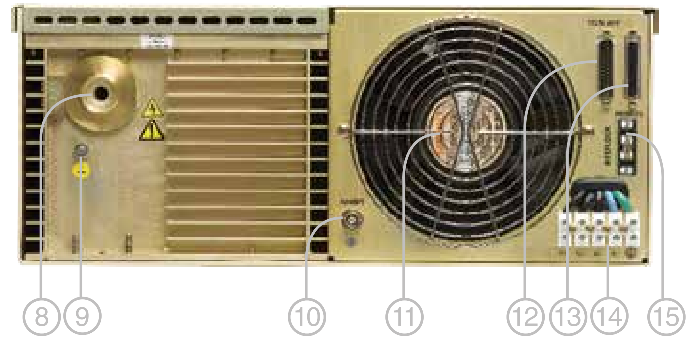
- **Power rating of 4kJ/sec, 5kJ/sec peak**
- **Output Voltages from 0-1kV to 0-50kV**
- **Compact air cooled rack mount package**
- **Efficient IGBT based resonant inverter**
- **Excellent pulse to pulse repeatability**
- **208 or 400VAC 3Ø input voltage**
- **Comprehensive remote control interface**
- **UL Approved AC line contactor (optional for OEM models)**
- **Ultra reliable and rugged industry standard design**
- **Passive PFC (pf = 0.85)**
- **Full local output voltage and HV On/Off controls (L version)**
- **Simple parallel operation for higher power**
- **Lab, Slave, or OEM front panel options**

Average Capacitor Charging Power	4,000 Joules/sec (½CV^2 x Rep Rate)
Peak Capacitor Charging Power	5,000 Joules/sec (½CV^2/t_{charge})
Average Continuous DC Power	4,000 Watts
Output Voltage Range	1, 2, 4, 5, 10, 15, 20, 30, 40, 50kV, variable from 10-100% of rated
Polarity	Available as fixed Positive or Negative. Please specify at time of ordering
HV Output Cable	1-39kV Models - DS2124 Coaxial cable with proprietary HV connector
	40-50kV Models - DS2214 Coaxial cable with proprietary HV connector
HV Insulating Medium	Exxon Mobil Univolt N61B or equivalent insulating oil
AC Input Voltage	208VAC (180-264), 3Ø or 400VAC (340-460), 3Ø + N, specify at time of ordering
AC Input Current	20A/15A
AC Connector	UL/CSA approved terminal block. 3Ø + ⏚ for 208VAC, 3Ø + N + ⏚ for 400VAC
AC Line Contactor	UL/CSA approved AC line contactor (standard on 402L and 402S, option for 402OEM)
Power Factor	Passive PFC pf = 0.85 at full load and nominal AC line
Efficiency	Better than 85% at full load
Front Panel	402L - Voltage Control, Voltage & Current Meters, Status Indicators
	402S - On/Off Switch, Status Indicators
	402-OEM - Blank front panel
Stability	0.2% per hour after 1 hour warmup
Temperature Coefficient	100ppm per °C typical
Stored Energy	Less than 0.3J all models
Pulse to Pulse Repeatability	±2% to 1000Hz, consult factory for higher rep rates
Dimensions - inches (mm)	19 (483) W x 7 (178) H x 17 (432) D
Weight - lbs (kg)	65 (30)
Ambient Temperature	Storage: -40 to +85°C. Operating: -20 to +45°C
Altitude	Storage: 40,000ft (12,000m), Operating: 9,900ft (3,000m)
Humidity	10-90%, non-condensing
Protection	Open/short circuits, Overloads, Arcs, Overtemp, Overvoltage, Safety Interlock
Remote Control (all models)	Via 25-pin D-sub connector on rear of unit, Signals include, Vprogram (0-10V), HV Enable/Reset, Inhibit, Summary Fault, Load Fault, Vanalog, Vpeak
Accessories	10ft HV cable, operating manual
Options	EN - Low Enable. Replaces standard high enable
	5V - 0-5V Analog programming. Replaces standard 0-10V programming.
	LP - Latching Overload Protection, requires HV reset after overload fault
	DC - Continuous DC operation
	CT - AC line contactor (option for 402OEM models only, standard on 402L and 402S)
	Double terminated HV cable, and mating bulkhead connector
Ordering Info	Model - XXkV - POS (or NEG) - YYYVAC - ZZ (options)
Ordering Examples	402L-10kV-POS, 402S-1kV-NEG-DC, 402-OEM-50kV-POS-400VAC
All specifications subject to change without notice	

402 Series Mechanical Details

402L Front View

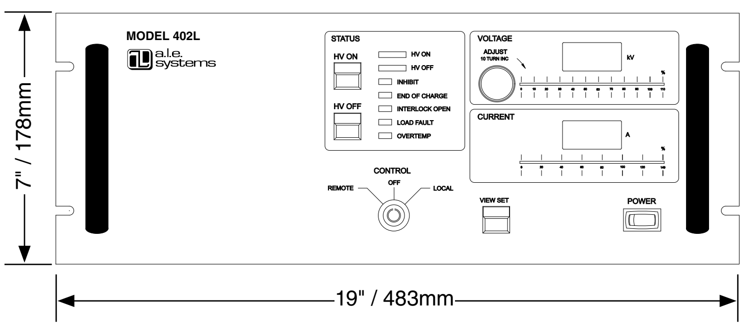
402L Rear View

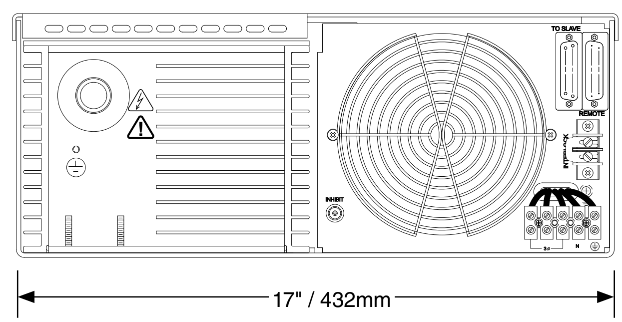


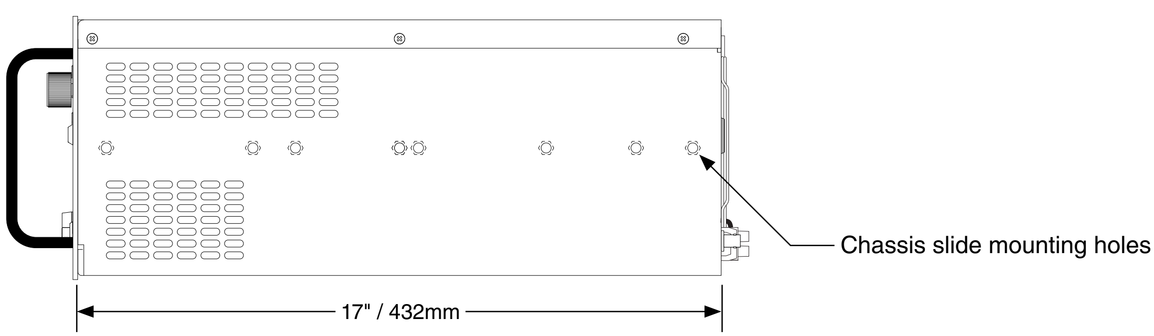
1 - HV On/Off Push Buttons (L model only)
2 - Status Indicator LEDs (L and S models only)
3 - Local/Remote Keyswitch (L model only)
4 - 10-Turn HV Output Control (L models only)
5 - View Set Push Button (L models only)
6 - Output Voltage and Current Displays (L models only)
7 - Power Switch (L and S models only)

8 - HV Output Connector
9 - Ground Stud
10 - Inhibit BNC (L models only)
11 - Cooling Fan
12 - Slave Supply Programming Connector (L models only)
13 - Remote Programming Connector
14 - AC Input Terminal Block
15 - Interlock Terminals (L and S models only)

Outline Drawings







Notes:

1 - Chassis slide mounting pattern matches General Devices CT series or equivalent with 3.875" hole spacing.

2 - Cooling air enters rear of unit and exits at either side. Do not block air vents or cooling fan and allow several inches of clearance at rear of unit.

3 - Allow 6" bend radius at rear of unit for HV cable.

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93 008 009 Rev G

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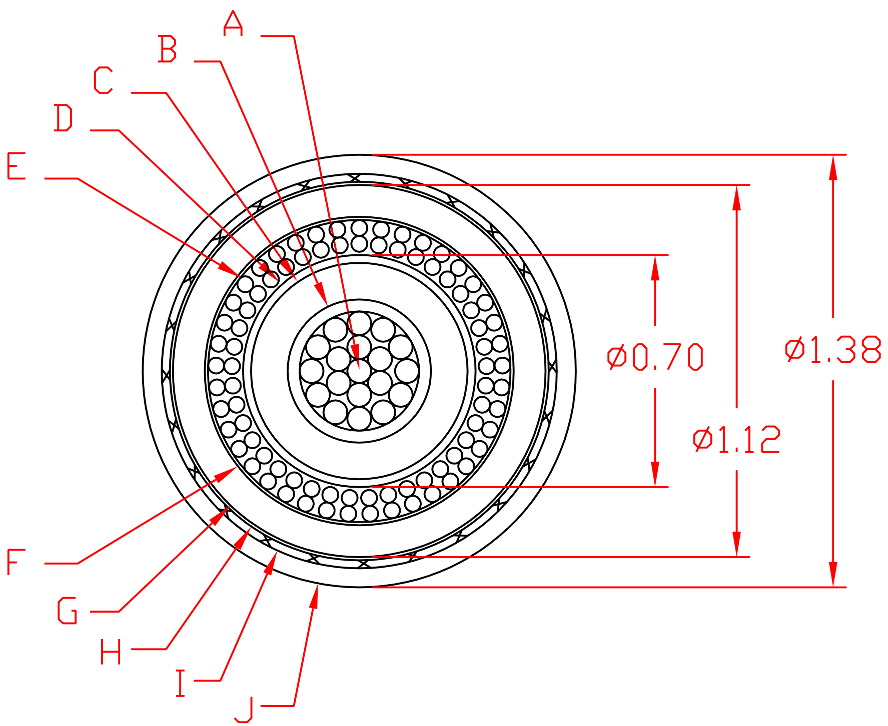
DWG NO.	REV
SK160114	1



LEGEND

A. #00 (19 X BARE COPPER COMPACTED), NOMINAL ø 0.376

B. SEMICONDUCTING EPR, ø 0.42

C. INSULATING EPR – ø 0.115 WALL TO ø0.65

D. SEMICONDUCTING EPR, ø 0.70

E. OUTER CONDUCTOR, DOUBLE LAYER, 12 INCH LAY
RHL INNER 41 x #18 AWG (19 x 30AWG T.C.)
LHL OUTER 41 x #18 AWG (19 x 30AWG T.C.)

F. SEMICON TAPE, 2" WIDE, 0.005 THK

G. INSULATING LDHMW POLYETHYLENE 0.100 WALL.

H. SEMICON TAPE, 2" WIDE, 0.005 THK

I. BRAID, #28 AWG T.C., 6 ENDS, 24 CARRIER, 70% COVERAGE.

J. JACKET, PVC, BLACK, 0.06 WALL.

REVISIONS			
REV	ECO NUMBER	APPD	DATE

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES
TOLERANCE ON

DECIMALS	ANGLES
.XX ±.01 .XXX ±.005	±

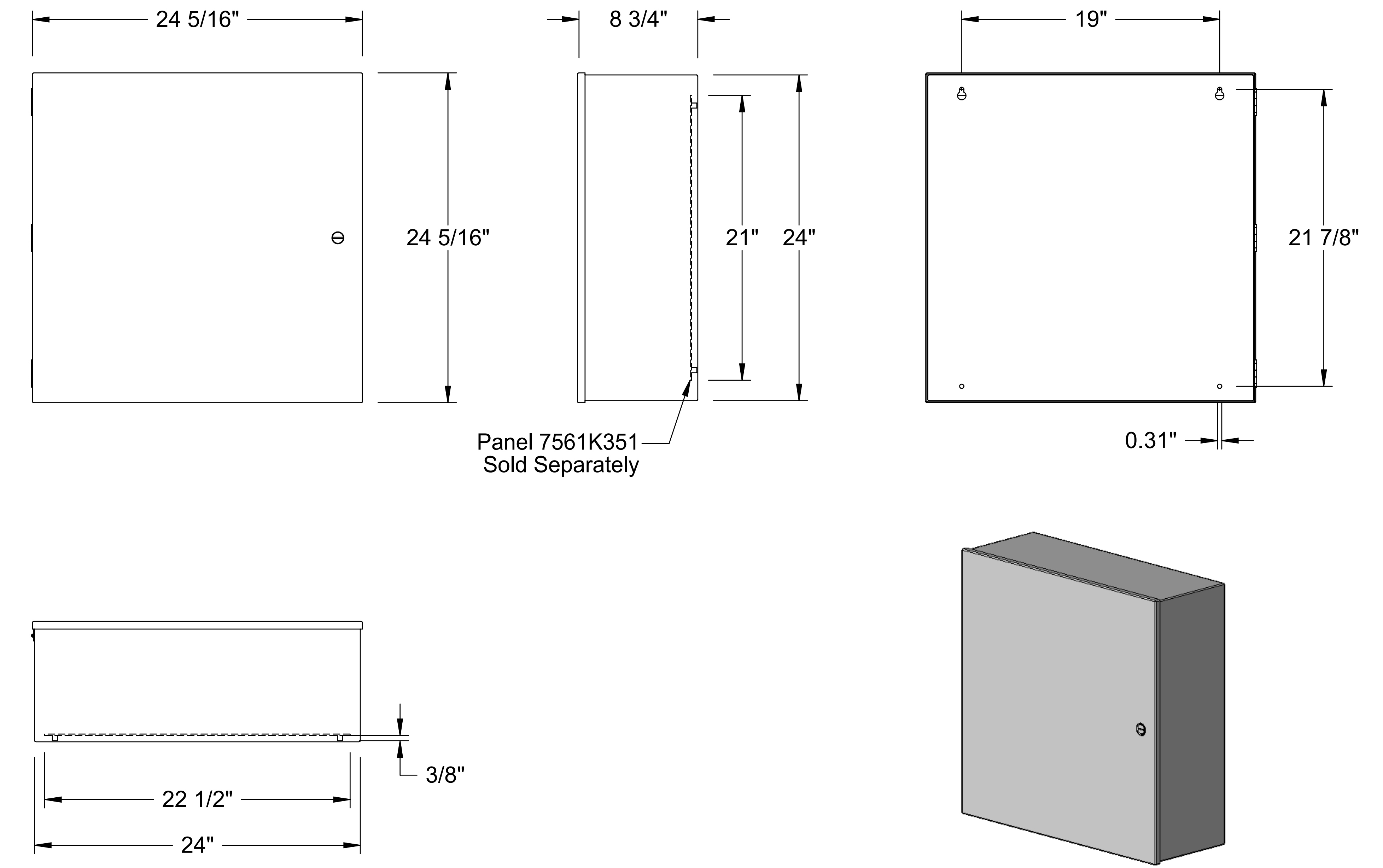
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINE SURFACES 125√

DRAWN D. ABDULKY	DATE 14JAN16
CHECKED	DATE
APPROVED	DATE
MATERIAL	
FINISH	

DIELECTRIC SCIENCES,INC
CHELMSFORD, MASSACHUSETTS 01824

HV CABLE

SIZE	FSCM NO.	DWG NO.	REV
A	50509	SK160114	1
SCALE		SHEET OF	



14-ga Steel (0.0747")
Approximate Internal Dimension: Ht. 23", Wd. 23", Dp. 8 1/8"

McMASTER-CARR® CAD	PART NUMBER	7561K64
http://www.mcmaster.com © 2014 McMaster-Carr Supply Company	Indoor Steel Enclosure	
Information in this drawing is provided for reference only.		